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Design of a Digital Temperature Sensor based on Thermal Diffusivity in a Nanoscale CMOS Technology

Dissertação para obtenção do Grau de Mestre em Engenharia Electrotécnica e de Computadores

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Universidade Nova de Lisboa

Resumo

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Electrotécnica e de Computadores

Dissertação para obtenção do grau de Mestre em

Engenharia Electrotécnica e de Computadores

por Roman Kliko

Sensores de temperatura são amplamente utilizados em microprocessadores para monitorizar gradientes de temperatura ‘on-chip’ e 'hot-spots', que são conhecidos por afectar negativamente a fiabilidade. Estes sensores devem ser pequenos, por razões de incorporação no circuito integrado do sistema, rápidos em detectar alterações térmicas transitórias em fracções de segundos, e de fácil ajuste para reduzir custos associados. Recentemente, foi demonstrado que sensores de difusividade térmica (TD) conseguem satisfazer esses requisitos. Esses sensores operam através da digitalização do atraso, dependente da temperatura, associado com a difusão de pulsos de calor através de um filtro electrotérmico (ETF), que, em tecnologia CMOS padrão, podem ser facilmente implementados como aquecedor resistivo cercado por uma termopilha. Ao contrário dos sensores de temperatura baseados em BJTs, as suas precisões na realidade melhoram com o escalamento dos transístores nas tecnologias CMOS, uma vez que é principalmente limitado pela precisão do espaçamento do aquecedor/termopilha.

Neste trabalho é apresentado um sensor TD altamente digitalizado em tecnologia CMOS de 0.13 μm com ± 1.5 ºC (3σ, ajuste único) de imprecisão e alcançando uma resolução melhor do que 1 ºC a uma taxa de amostragem da ordem de 1 kS/s, e que se compara favoravelmente aos sensores de última geração com precisão similar e taxas de amostragem [1][2][3][4]. Este avanço é alcançado nomeadamente pela adoção de uma arquitectura de modulação $\Sigma\Delta$, altamente digital, baseado num oscilador controlado por corrente (CCO).

O sensor TD apresentado consiste num ETF, num andar de trasnconductância, num oscilador controlado por corrente (CCO) e num contador digital de 6 bits.

De modo a ser facilmente portado para tecnologias CMOS de escala nanométrica, é proposto usar um modulador sigma-delta baseado num CCO como uma alternativa aos moduladores tradicionais. Dado que 70% da área do sensor é ocupada por circuitos puramente digitais, portar o sensor para tecnologia CMOS de última geração deve reduzir substancialmente a área digital, e assim reduzir significativamente a área total do sensor.

Palavras-Chave: Sensor de Temperatura Digital, Difusividade Térmica, Gestão Térmica Dinâmica, Filtro Electrotérmico, Modulação Sigma-Delta, Oscilador Controlado por Corrente.

Universidade Nova de Lisboa

Abstract

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Electrotécnica e de Computadores

Dissertação para obtenção do grau de Mestre em

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by Roman Kliko

Temperature sensors are widely used in microprocessors to monitor on-chip temperature gradients and hot-spots, which are known to negatively impact reliability. Such sensors should be small to facilitate floor planning, fast to track millisecond thermal transients, and easy to trim to reduce the associated costs. Recently, it has been shown that thermal diffusivity (TD) sensors can meet these requirements. These sensors operate by digitalizing the temperature-dependent delay associated with the diffusion of heat pulses through an electro-thermal filter (ETF), which, in standard CMOS, can be readily implemented as a resistive heater surrounded by a thermopile. Unlike BJT-based temperature sensors, their accuracy actually improves with CMOS scaling, since it is mainly limited by the accuracy of the heather/thermopile spacing.

In this work is presented the electrical design of an highly digital TD sensor in 0.13 μm CMOS with an accuracy better than 1 ºC resolution at with 1 kS/s sampling rate, and which compares favourably to state-of-the-art sensors with similar accuracy and sampling rates [1][2][3][4]. This advance is mainly enabled by the adoption of a highly digital CCO-based phase-domain ΔΣ ADC.

The TD sensor presented consists of an ETF, a transconductance stage, a current-controlled oscillator (CCO) and a 6 bit digital counter.

In order to be easily ported to nanoscale CMOS technologies, it is proposed to use a sigma-delta modulator based on a CCO as an alternative to traditional modulators. And since 70% of the sensor's area is occupied by digital circuitry, porting the sensor to latest CMOS technologies process should reduce substantially the occupied die area, and thus reduce significantly the total sensor area.

Keywords: Digital Temperature Sensor, Thermal Diffusivity, Dynamic Thermal Management, Electro-thermal Filter, Sigma-Delta Modulation, Current-Controlled Oscillator.

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Acronyms and Abbreviations

TD	***T**hermal **D**iffusivity*
TDT	***T**hermal **D**iffusivity **T**emperature*
TDC	***T**emperature-to-**D**igital **C**onverter*
ETF	***E**lectro-**T**hermal **F**ilter*
VCO	***V**oltage-**C**ontrolled **O**scillator*
CCO	***C**urrent-**C**ontrolled **O**scillator*
CMOS	***C**omplementary **M**etal-**O**xide-**S**emiconductor*
BJT	***B**ipolar **J**unction **T**ransistor*
NPN	***N**egative **P**ositive **N**egative*
PNP	***P**ositive **N**egative **P**ositive*
ADC	***A**nalog-to-**D**igital **C**onverter*
DAC	***D**igital-to-**A**nalog **C**onverter*
DTM	***D**ynamic **T**hermal **M**anagement*
MOSFET	***M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor*
DC	***D**irect **C**urrent*
FET	***F**ield-**E**ffect **T**ransistor*
YIT	***Y**ttrium **I**ron **G**arnet*
SAW	***S**urface **A**coustic **W**ave*
MSB	***M**ost **S**ignificant **B**it*
LSB	***L**east **S**ignificant **B**it*
FSR	***F**ull **S**cale **R**ange*
SOI	***S**ilicon **O**n **I**nsulator*
DEM	***D**ynamic **E**lement **M**atching*
SAR	***S**uccessive **A**pproximation **R**egister*
RFID	***R**adio **F**requency **ID**entification*
CDS	***C**orrelated **D**ouble **S**ampling*
PTAT	***P**roportional **t**o **A**bsolute **T**emperature*

Chapter

1

Introduction

1.1. Background and Motivation

Temperature sensors are broadly used in microprocessors to control on-chip temperature gradients and hot-spots, known to negatively impact reliability [1][2][3][4]. With microprocessors scaling to higher performance and faster speed, heat dissipation has become a growing concern. Excessive heat degrades performance and increases power dissipation of the entire system [6]. When microprocessors getting hot, the cooling system must handle worst-case workloads, having as solution, dynamic thermal management (DTM), which enables dynamically balanced workload, the cooling system only has to handle average workloads, and the need to integrate temperature sensors. Such temperature sensors should be: 1) small to facilitate floor planning; 2) fast to track millisecond thermal transients; 3) easy to trim to reduce the associated costs and 4) have efficient DTM to be accurate [5].

In Fig.1.1 is presented the block diagram of the thermal diffusivity temperature sensor that is designed and discussed in this thesis. It includes a CCO-based phase-domain ΔΣ modulator with the accompanying timing diagram to a better understanding its operation.

As general trend, CMOS sensors are less accurate sensors. Thermal diffusivity (TD) sensors scale better, but are large and analog. Therefore, the objective is to make TD sensors small and with more digital content. Speed of heat pulses in Si substrate is temperature dependent, so, periodic heat signals will be phase-shifted by Φ(T). The benefits from CMOS technology are the: 1) high purity silicon, which enables a well-defined thermal diffusivity, 2) accurate lithography, which allows a well-defined spacing between heater and heat detector and 3) fast circuitry, to assure more accurate read-out of the delay.

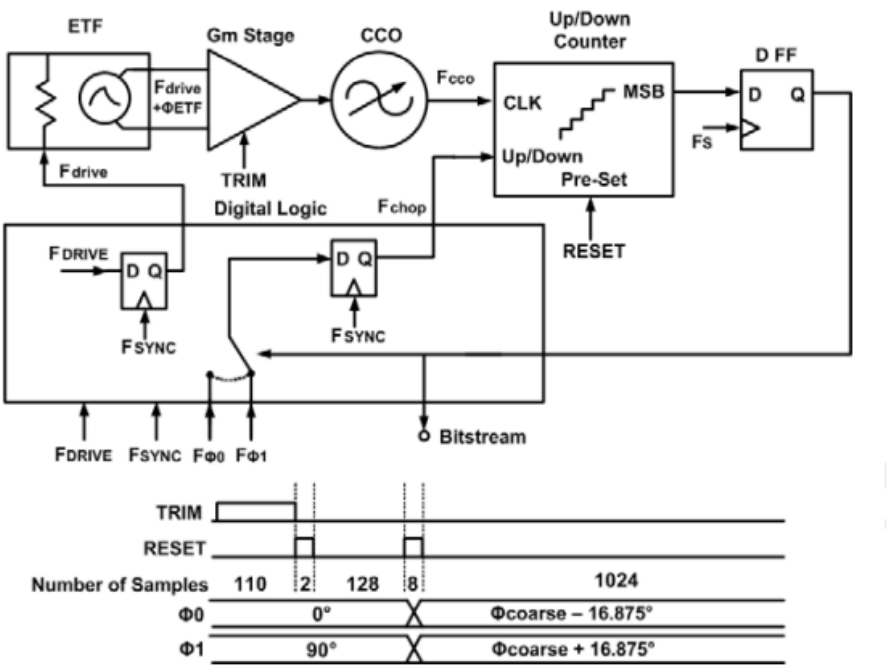

Figure 1.1 – Block diagram of the proposed thermal diffusivity temperature sensor with a CCO-based phase-domain ΔΣ modulator, and the corresponding timing diagram [48].

The operation of TD sensors is based on the measurement of *D*, the thermal diffusivity of silicon. Regarding to this type of sensors, the temperature dependence of *D* is well-defined and the same is insensitive to process spread, in IC-grade silicon. By measuring the thermal delay between an on-chip heater and an on-chip relative temperature sensor, can be found the parameter *D*. Posteriorly, this delay can be digitized or used in order to define the output frequency of an oscillator. Also, was discovered that the inaccuracy of TD sensors scales with process technology and is insensitive to mechanical stress [7].

The use of integrated temperature sensors for temperature control and thermal management has become popular in the last few decades [8]. CMOS temperature sensors are found in many consumer and industrial applications, as a result of their low cost and facility of use. The majority of the CMOS temperature sensors are based on the well-known temperature dependence of bipolar transistors or diodes. But, the untrimmed inaccuracy of such sensors is limited to a few degrees Celcius, by process spread. The inaccuracy of such sensors can be reduced to the order of $\pm$0.25 ºC (3σ) over the military temperature range (-55 to 125 ºC), after batch calibration [9], and by individual trimming at a single temperature, it can be improved to $\pm$0.1 ºC (3σ) [10]. The problem is that, individual trimming of packaged devices is costly and time-consuming. Instead, can be used wafer level trimming, that is easier, while the mechanical stress associated with packaging can induce to an presentation of several tenths of a degree of 'packaging swap' by BJT-based sensors [11]. Besides, the inaccuracy of BJT-based sensors in deep sub-micron CMOS, has not evolved [12][13][14], compared to older projects of designs [9]. Yet, there has been made a

few recent projects using MOSFET-based sensors, presenting inaccuracies of -0.4/+0.6 ºC over a 100 ºC range after two-temperature trimming, showing worst inaccuracies than that of BJT-based sensors [15]. In order to overcome this situation, has appeared a promising alternative, based on the measurement of the thermal diffusivity of bulk silicon, *D*, being a strong function of absolute temperature *T*, and approximately proportional to $1/T^{1.8}$ [16][17]. *D* can be determined by measuring the time it takes for a small amount of heat to diffuse from an on-chip heater to a neighbouring relative temperature sensor, usually a thermopile, as can be seen in Fig. 1.2. This type of structure is known as an electro-thermal filter (ETF), where the heat signal is affected by the delay and attenuation in the diffusivity process through the substrate. *D* is very well-defined, for a highly pure IC-grade silicon, and the spacing between the heater and the thermopile, *s*, is accurately determined by lithography, resulting in characteristics that are well-defined and low untrimmed inaccuracy, of thermal diffusivity (TD) sensors.

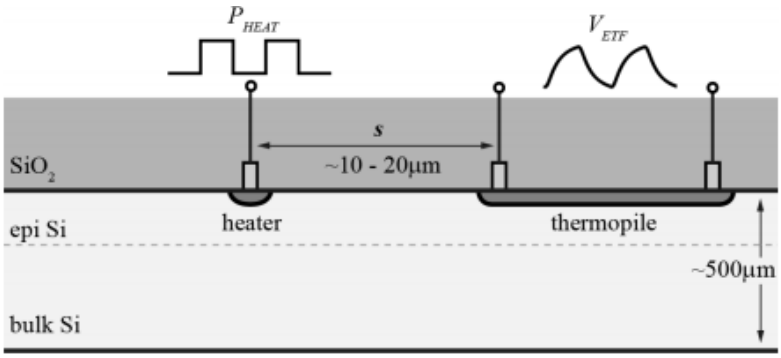

Figure 1.2 – Lateral view of an Electrothermal Filter (ETF) in bulk CMOS technology [43].

The inaccuracy of these TD sensors scales with the technology scaling-down, and for that reason, they are appropriate for the thermal management of microprocessors and for high-temperature applications (>190 ºC), since they will not be affected by leakage currents.

1.2. Main Objectives

In this section is defined a brief summary of the majority of the chapters presented in this work, showing the most important topics, and the structure of the thesis. This document is constituted by five chapters, describing the block-diagram of the thermal–diffusivity temperature sensor system, the design and sizing, the electrical simulations of the individual building-blocks and of the complete system. Conclusions are drawn in the last chapter.

1.3. Thesis Outline

Chapter 2 – State-of-the-Art of Temperature Sensors

In this chapter will be presented some temperature sensor architectures, enunciating its technical characteristics and differences between them. In the end will be presented a comparative table with performance summary.

Chapter 3 – Design of the Main Building-Blocks

The third chapter focuses on the study of the Thermal-Diffusivity Temperature Sensor circuit, analysing each block individually, describing its operation, accompanied by illustrative figures, and always including the theoretical analysis.

Chapter 4 – Design Methodology and Sizing

The adopted final dimensions of the transistors will be shown in this chapter, presenting the size procedure, to provide a better insight of the choices made, and how they can affect the behaviour of the circuit, in order to meet the desired specifications. This chapter will be divided into two sections, the first one discusses the digital part of the final TDT Sensor circuit, and, the second one, will describe the analog part of the final TDT Sensor circuit.

Chapter 5 – Simulation Results

This chapter summarizes the final results obtained from many electrical simulations carried out throughout this work, showing graphics, their analysis and comments about the results. The simulation strategy comprises several steps, which will be presented in incremental way, successively adding blocks to the final Thermal-Diffusivity Temperature Sensor circuit, in order to better understand the final adopted dimensions of the elements in each block and the current that feeds some of them.

Chapter 6 – Conclusions and Future Work

In this last chapter some discussion is provided to summarize the main conclusions about the whole project, in order to be possible realize future development and research about the studied and described sensor.

1.4. Thesis Contributions

It is expected that the work developed in this thesis can be helpful in the design, sizing and development of the new generation of thermal-diffusivity temperature sensors, using the most recent transistor scaling dimensions, and thereby dramatically decreasing the area occupied by this type of sensors.

Chapter 2

State-of-the-Art of Temperature Sensors

In the present chapter, the most competitive temperature sensor architectures are presented.

Temperature sensors are largely used in electronic circuits, in order to measure their temperature. With the passage of years, these sensors have evolved, using different types of technology ranging from a solid 0.7 μm to a modern 22 nm CMOS technologies. The different types of sensors can be categorized in BJT, NPN, PNP, Diode, Delay, and TD, with different inaccuracies (3σ), temperature ranges, silicon areas, and power consumptions.

The temperature sensor presented in this thesis is a derivation from other similar temperature sensors, but with different operating principles.

2.1. Sensor types

2.1.1. Sensors based on PNP Devices

As a comparison example, its possible to start with a smart temperature sensor designed, fabricated and experimentally evaluated in an old 0.7 μm CMOS with a 3σ inaccuracy of a $\pm$0.1 ºC over the full military temperature range of -55 ºC to 125 ºC, using substrate PNP transistors to provide the temperature sensing [39]. The errors resulted from non-idealities in a readout circuitry are decreased to the 0.01 ºC level, achieved by using dynamic element matching (DEM), a chopped current-gain independent PTAT bias circuit, and a low-offset second-order sigma-delta ADC combining both, chopping and correlated double sampling techniques. Based on a calibration at one temperature, trimming is able to compensate for the spread of the base-emitter voltage characteristics of the substrate PNP transistors. Moreover, it is used a sigma-delta current-mode DAC to fine-tune the bias current of the bipolar transistors, in order to obtain a high trimming resolution [39].

In a 0.16 μm CMOS technology, a temperature sensor for RFID applications has been described in [40]. The PNP-based sensor uses a digitally-assisted readout scheme that helps decreasing the area and the associated complexity of the analog circuitry, with trimming simplification. The main characteristic of this project is an energy-efficient two-step zoom ADC combining a coarse 5-bit SAR conversion with a fine 10-bit $\Sigma\ \Delta$ conversion. After a single trim at 30 ºC is achieved by the sensor an inaccuracy of $\pm$0.2 ºC (3σ) from -30 ºC to 125 ºC and a resolution of 15 mK at a conversion rate of 10 Hz. The area occupied by the sensor is only 0.12 mm^2 drawing a current of 4.6 μA from 1.6 V to 2 V supply, corresponding to a very small power dissipation of 7.4 μW [40].

2.1.2. Sensors based on NPN Devices

In a more advanced 65 nm CMOS process is presented an NPN-based temperature sensor with digital output, achieving a batch-calibrated inaccuracy of $\pm$0.5 ºC (3σ) and a trimmed inaccuracy of $\pm$0.2 ºC (3σ) over the temperature range from -70 ºC to 125 ºC. In this project are used the NPN transistors as sensing elements, the use of dynamic techniques as correlated double sampling (CDS) and dynamic element matching (DEM), and a single room-temperature trim, in order to obtain this type of performance. The area occupied by this sensor is only 0.1 mm^2, drawing a current of 8.3 μA from a 1.2 V supply [41].

2.1.3. Standard BJT Sensors

Another temperature sensor for RFID temperature sensing usage relies on a low power, energy-efficient smart temperature sensor in 0.16 μm CMOS technology. It is a BJT-based sensor, employing an energy-efficient 2nd-order (incremental) zoom ADC, combining a coarse 5-bit SAR conversion with a fine 10-bit $\Delta\ \Sigma$ conversion. The conversion time is halved by a new integration scheme, with no additional supply current. A fast voltage calibration technique that can be carried out in only 200 msec, is used, in order to meet the stringent cost constraints on RFID tags. This sensor can achieve an inaccuracy of $\pm$0.15 ºC (3σ) from -55 ºC to 125 ºC, after batch and an individual room-temperature calibration. Devices from a second lot can achieve an inaccuracy better than $\pm$0.25 ºC (3σ) in both ceramic and plastic packages, over the same temperature range. The sensor occupies only 0.08 mm^2, drawing a current of 3.4 μA from a 1.5 V to 2 V supply, and achieving a resolution of 20 mK in a conversion time of 5.3 msec, corresponding to a minimum energy dissipation of 27 nJ per conversion [42].

2.1.4. Temperature Sensors based on Thermal diffusivity

A temperature sensor similar to the one studied and designed in this work is the temperature sensor based on the measurement of the thermal diffusivity of silicon *D*. The advantage of this type of sensors is that in IC-grade silicon, *D* has a well-defined temperature dependence, is insensitive to process spread, and can be determined by measuring the thermal delay between an on-chip heater and an on-chip relative temperature sensor, where this delay can posteriorly be digitized or used to define the output frequency of an oscillator. This thermal diffusivity (TD) sensor has been fabricated in 0.7 μm and 0.18 μm bulk CMOS, and in a 0.5 μm SOI technology, wherein its outputs are well-defined functions of temperature and can work over a temperature range from -70 ºC to 170 ºC. Morever, it was discovered that the inaccuracy of TD sensors scales proportionally with process technology scaling and is insensitive to mechanical stress. And with an implementation in 0.18 μm bulk CMOS could be achieved an untrimmed inaccuracy of the order of ± 0.2 ºC (3σ) from -55 ºC to 125 ºC [43].

Another similar temperature sensor to the studied in this work is a temperature sensor based on thermal diffusivity sensing, realized in 0.7 μm CMOS technology, presenting characteristics as insensitivity to leakage currents, allowing a reliable operation beyond 150 ºC. And as thermal diffusivity sensors have low intrinsic spread, they do not require expensive trimming in many applications. The untrimmed device-to-device spread corresponds to a temperature error of ± 0.7 ºC (3σ) with a big operating range from -70 ºC to 160 ºC, featuring a significant improvement on the state-of-the-art [44].

One of the way to read out the temperature by the sensors is through an Electro-Thermal Filter (ETF), and for this purpose can be used a CMOS temperature-to-digital converter (TDC), that operates measuring the temperature-dependent phase shift of an ETF, where the layout of this important block has been optimized to minimize the thermal phase spread caused by lithographic inaccuracy. The TDC's front-end consists of a wide bandwidth gain-boosted transconductor in order to minimize the electrical phase spread. Posteriorly, is digitized the transconductor's output current by a phase-domain $\Sigma\,\Delta$ modulator whose phase-summing node is realized by a chopper demodulator. The demodulator is located at the virtual ground nodes established by the transconductor's gain-boosting amplifiers, to minimize the residual offset caused by the demodulator's switching action. After measuring 16 different samples, it can be concluded that the TDC has an untrimmed inaccuracy better than ± 0.7 ºC (3σ) over the military range, variyng from -55 ºC to 125 ºC [45].

2.1.5. Results comparison

For a better understanding of the major differences involved in the different types of temperature sensors described so far, an informative table (Tab.2.1) is presented next with their most relevant key performance parameters.

Table 2.1: Performance summary and comparison with other state-of-the-art sensors reported in the literature.

	[39]	[40]	[41]	[42]	[43]	[44]	[45]
Technology	0.7 μm	0.16 μm	65 nm	0.16 μm	0.18 μm	0.7 μm	0.7 μm
Sensor Type	BJT	BJT	BJT	BJT	TD	TD	TD
Inaccuracy (3σ)	$\pm$0.1ºC	$\pm$0.2ºC	$\pm$0.2ºC	$\pm$0.15ºC	$\pm$0.2ºC	$\pm$0.7ºC	$\pm$0.7ºC
Temp. Range	-55ºC - 125ºC	-30ºC - 125ºC	-70ºC - 125ºC	-55ºC to 125ºC	-55ºC to 125ºC	-70ºC to 160ºC	-55ºC to 125ºC
Area (mm^2)	4.5 mm^2	0.12 mm^2	0.1 mm^2	0.08 mm^2	-	-	2.3 mm^2
Power	-	7.4 μW	-	-	-	-	5 mW

Chapter

3

Design of the Main Building-Blocks

In the present chapter, the design of a thermal-diffusivity temperature sensor with an embedded CCO-based phase domain ΔΣ modulator will be presented. All main components of this sensor will be described, and included, later on, in the composition of the final block diagram of the complete sensor system.

The circuit of this thermal-diffusivity temperature sensor is composed by a digital part (comprising *D* and *JK* flip-flops, a 6 bit counter, and several NMOS, PMOS and CMOS switches), and by an analog part (comprising a current-controlled oscillator (CCO), a transconductance stage (*gm*), a 6 bit current-mode DAC (IDAC) and an electro-thermal filter (ETF)), as can be seen in Fig.3.1.

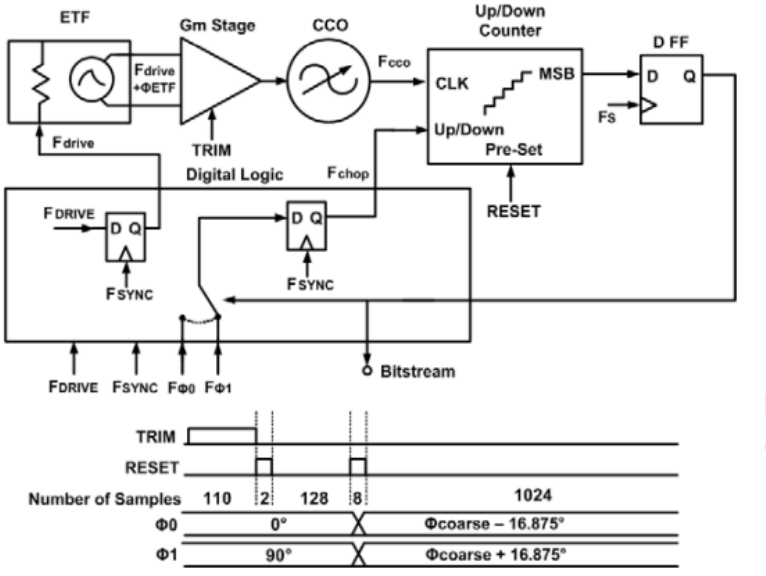

Figure 3.1 – Block diagram of the proposed thermal diffusivity temperature sensor with a CCO-based phase-domain ΔΣ modulator, and the corresponding timing diagram [48].

3.1. Flip-Flops

Flip-flops and latches are used as data storage elements. They are the basic memory elements used in clocked sequential circuits. Such circuits are binary cells with capacity to store one bit of information. It has two outputs, first for the normal value and the second for the complement value of the bit stored in it. There are many ways where binary information can enter a flip-flop.

A flip-flop has an important characteristic, the output can exist in one of the two stable states, logic 1 and logic 0, simultaneously, which is supported by the appropriate crossed feedback connections associated with the most common form of flip-flop called as a latch.

Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems. Computers use huge amounts of flip-flops, creating a need to coordinate their working, through a square wave signal known as clock signal (CLK) that is applied to the flip-flop, preventing the flip-flop from changing state until the right instant occurs [34].

There are many types of flip-flops, as *D*, *JK*, *RS* and *T* flip-flops, that are also called "latches", "bistable multivibrators", or "binaries". Functional flip-flops can be made from logic gates, or be available in IC form. They are connected to form sequential logic circuits for data storage, counting, timing and sequencing [19].

The major difference between a latch and a flip-flop, is that a latch is a sequential circuit that changes their outputs depending on inputs, without any intervention of clock. While a flip-flop is a sequential circuit more controllable, that changes their outputs only by the action of clock [21].

One of flip-flop's characteristics is that if a flip-flop circuit is always provided with power, it can maintain a binary state indefinitely until directed by an input signal to switch states. The number of inputs and the manner, in which the inputs affect the binary state, are the biggest differences among various types of flip-flops [18][20].

3.1.1. *D* Flip-Flop

The logic symbol for a common type of flip-flop is shown in Fig. 3.2. The *D flip-flop* has only a single *data* input (*D*) and a clock input (CLK). The customary *Q* and *Q'* outputs are shown on the right side of the symbol. The *D flip-flop* is often called a *delay flip-flop*. This name accurately describes the unit's operation. Whatever the input at the data (*D*) point, it is *delayed* from getting to the normal output (*Q*) by *one clock pulse*. Data is transferred to the output on the transition of the clock pulse [19].

The *D* flip-flop receives the designation from its ability to hold *data* into its internal storage. The binary information present at the data input of the *D* flip-flop is transferred to the *Q* output when the *Clk* input is enabled. The output follows the data input as long as the pulse remains in its 1 state. When the pulse goes to 0, the binary information that was present at the data input at the time the pulse transition occurred is retained at the *Q* output until the pulse input is enabled again [18].

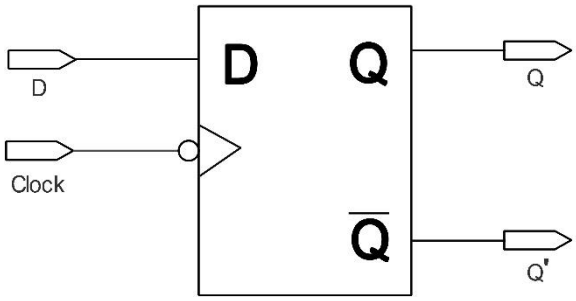

Figure 3.2 – Logic symbol for edge-triggered negative *D* flip-flop.

The *edge-triggered D* flip-flop is a modification of its *RS* counterpart [20]. It can be achieved replacing the *R* input with an inverted version of the *S* input, which thereby becomes *D*. This procedure is only done in the master latch section, leaving the slave unchanged, as presented in Fig. 3.3.

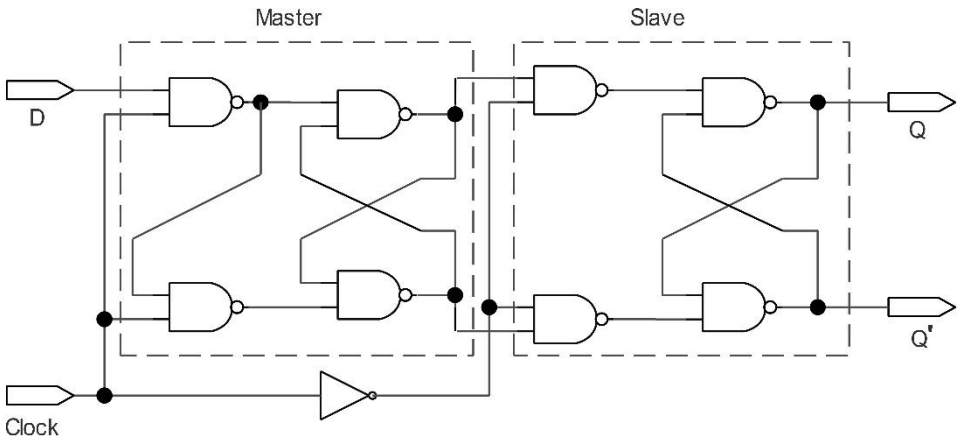

Figure 3.3 – Circuit schematic of a master-slave negative edge-triggered *D* flip-flop.

A master-slave *D* flip-flop is created by connecting two gated *D* latches in series, and inverting the *enable* input to one of them. It is called master–slave because the second latch in the series only changes in response to a change in the first (master) latch.

Observing the logic symbol for *D* flip-flop in Fig. 3.2, the clock (CLK) input has a small > inside the symbol, meaning that this is an *edge-triggered* device, and the presence of a bubble at the triangle means that this *D* flip-flop is *triggered* on the negative going edge [21].

This *ngative edge-triggered* flip-flop transfers data from input *D* to output *Q* on the HIGH-to LOW transition of the clock pulse, in other words, it is the *change of the clock* from HIGH to LOW (or H to L) that transfers data [19], as confirmed through the observation of the Tab. 3.1.

Table 3.1 – Truth table of a master-slave negative edge-triggered *D* flip-flop.

Inputs		Outputs		Comments
D	CLK	Q	Q´	
1	↓	1	0	Set
0	↓	0	1	Reset
X	0	Q_0	Q'_0	
X	1	Q_0	Q'_0	

In *negative edge-triggered* flip-flop the *Master* is running with CLK and *Slave* with CLK**'**, instead of *positive edge-triggered* flip-flop, where the *Slave* is controlled by CLK and *Master* by CLK**'**, as can be seen in Fig 3.4 and Fig. 3.5.

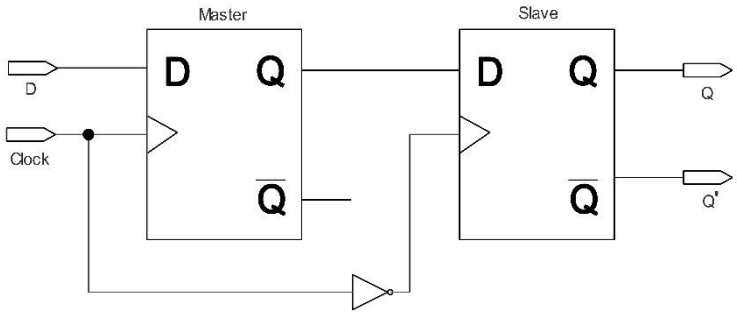

Figure 3.4 – Representation of a master-slave negative edge-triggered *D* flip-flop.

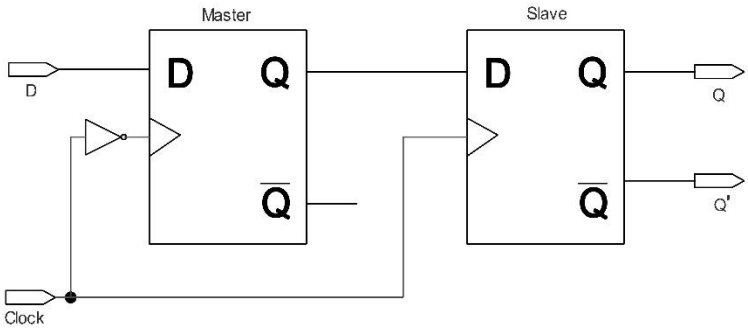

Figure 3.5 – Representation of a master-slave positive edge-triggered *D* flip-flop.

3.1.2. *JK* Flip-Flop

A *JK* flip-flop have similarities with *RS* flip-flop with the indeterminate state of the last one flip-flop being defined in the first one flip-flop, with the inputs *J* and *K* working like inputs *S* and *R* to set and clear the flip-flop. *Set* is controlled by input *J* and *reset* is controlled by input *K*, and when both inputs *J* and *K* are activated, the flip-flop changes to its complement state [18][20].

The *JK* flip-flop used in this project is a negative master-slave flip-flop with *set* and *clear*, constituted by two 2 input NAND gates, six 3 input NAND gates and one inverter, as can be seen in Fig. 3.6.

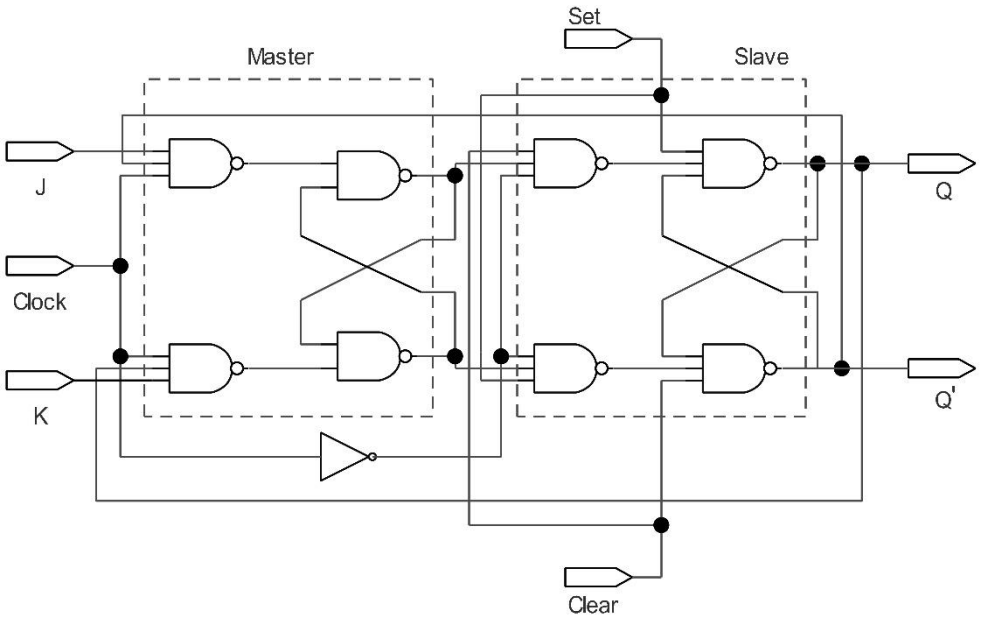

Figure 3.6 – Circuit schematic of master-slave negative *JK* Flip-Flop with *set* and *clear*.

3.2. The Digital Counter

Counters are important digital electronic circuits, and are used extensively in the design of digital systems and are classified as standard items [20]. They are sequential logic circuits because *timing* is important and they need a *memory* characteristic. *Digital counters* have some important characteristics as maximum number of counts (modulus of counter), up or down count, asynchronous or synchronous operation, and are free-running or self-stopping. As with other sequential circuits, flip-flops are used to construct counters [19].

A counter is essentially a register/sequential circuit that goes through a predetermined sequence of states upon the application of input pulses [20]. The gates in a counter are connected

in such a way as to produce a prescribed sequence of binary states in the register. Counters are extremely useful in digital systems, and can be used to count events such as a number of clock pulses in a given time (measuring frequency). They can be used to divide frequency and store data as in a digital clock, and they can also be used in sequential addressing, in some arithmetic circuits, and for generating timing variables to sequence and control the operations in a digital system [18][19].

3.2.1. Synchronous 6-bit Up/Down Binary Counter

In a synchronous counter, all flip-flops are triggered simultaneously by the counting clock pulse. As shown in the counter of this work, all Clk terminals are connected to the count pulse [20].

In a synchronous count-down binary counter, the flip-flop in the lowest-order position is complemented with every pulse. A flip-flop in any other position is complemented with a pulse provided all the low-order bits are equal to 0. For example, if the present state of a 6-bit count-down binary counter is $Q_6Q_5Q_4Q_3Q_2Q_1$ = 110000, the next count will be 101111. Q_1 is always complemented. Q_2 is complemented because the present state of Q_1 = 0. Q_3 is complemented because the present state of Q_2Q_1 = 00. Q_4 is complemented because the present state of $Q_3Q_2Q_1$ = 000. Q_5 is complemented because the present state of $Q_4Q_3Q_2Q_1$ = 0000. But Q_6 is not complemented because the present state of $Q_5Q_4Q_3Q_2Q_1$ = 10000, which is not an all-0's condition [18].

The counter used in this work/project is a synchronous 6-bit up/down binary counter presented in Fig. 3.7. Basing on analysis obtained through the simulation, when the *up/down* input control is 1, the circuit counts up, since the *J* and *K* inputs receive their signals from the values of the previous normal outputs of the flip-flops. When the *up/down* input control is 0, the circuit counts down, since the complemented outputs of the previous flip-flops are applied to the *J* and *K* inputs [18].

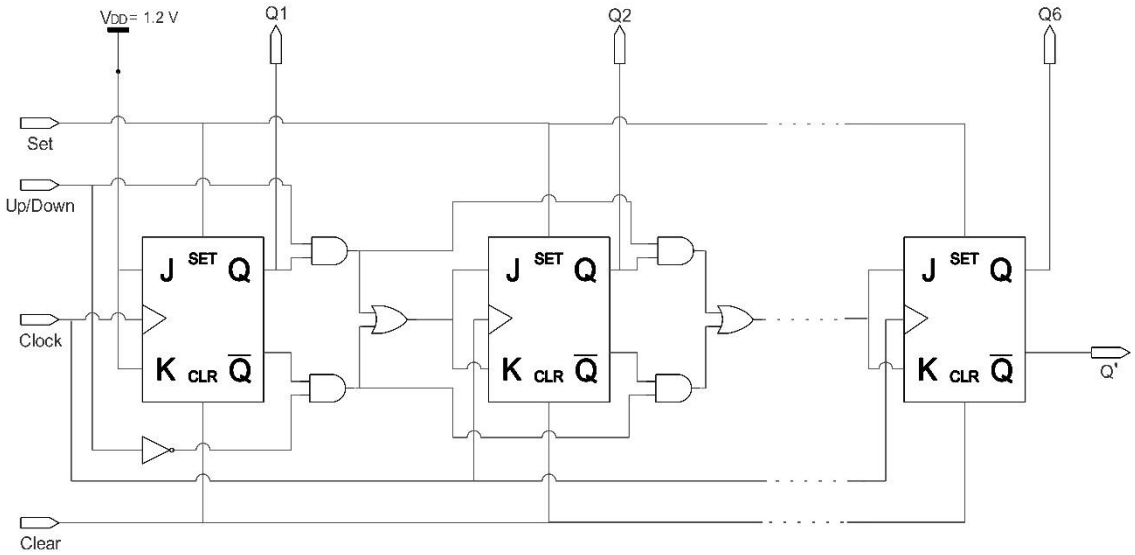

Figure 3.7 – Circuit schematic of synchronous 6 bit up/down binary counter.

3.3. Controlled Oscillators

Oscillators are an integral part of many electronic systems. In their design and construction different topologies and performance parameters are required, because of many applications that the same can have. Oscillators are normally embedded in a phase-locked system (PLL), and some of the challenges in their CMOS design are robustness and high-performance [29][30].

An electrical oscillator generates a periodically time-varying output signal (sinusoidal sine wave or square wave, saw-tooth or triangular shaped waveforms, or just a train of pulses of a variable or constant width) from DC power. As such, the circuit must involve a self-sustaining mechanism that allows its own noise to grow and eventually become a periodic signal [22].

An oscillator is basically an amplifier with positive feedback, or regenerative feedback (in-phase). There are many types of oscillators, various forms of oscillator implementations, and many different circuit configurations that produce oscillations; tuned-circuit oscillators (LC tuned oscillators, FET oscillators, BJT oscillators, op-amp oscillators, delay-line oscillators, voltage controlled oscillators), crystal oscillators (PI-network oscillators, ceramic-resonator oscillators, SAW oscillators), negative-resistance oscillators (dielectric-resonator oscillators, YIG oscillators), and non-sinusoidal oscillators (relaxation oscillators, ring oscillators, triangular-wave oscillators, saw-tooth oscillators, oscillators using 555 timer). Some oscillators produce sinusoidal signals, others produce non-sinusoidal signals. Sinusoidal oscillators are used in many applications, as in wireless systems, in consumer electronic equipment, and in test equipment. Non-sinusoidal oscillators, such as pulse and ramp/saw-tooth oscillators are used in timing and control applications. Pulse oscillators are normally found in digital-systems clocks, and ramp oscillators are found in the horizontal sweep circuit of oscilloscopes and television sets [23][27].

The feedback, that is one of the most important electrical engineering concepts, is approached in oscillator design. The feedback consists in add or subtract to the input variable of a system a quantity proportional to output variable [28].

The basic components in a feedback oscillator are the amplifier, an amplitude-limiting component, a frequency-determining network, and a (positive) feedback network. Normally the amplifier likewise acts as the amplitude-limiting component. The frequency-determining network often performs the feedback function. The feedback circuit is essential to return some of the output signal back to the input. Moreover, the positive feedback takes place when the feedback signal is in phase with the input signal. Once verified the necessary conditions, is possible to have oscillation [23]. In other words, an oscillator is an amplifier, which uses positive feedback that generates an output frequency without the use of an input signal. It is self-sustaining.

At start-up, however, oscillation is triggered by transients or noise, after which a properly designed oscillator will reach a stable oscillation state [25].

The presence of a loop at the core of any oscillator circuit causes a positive feedback at a selected frequency [26]. Fig. 3.8, provides the generic closed-loop system representation.

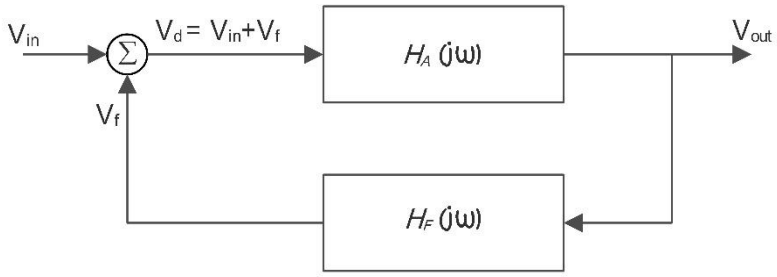

Figure 3.8 – Closed-loop circuit model of basic feedback oscillator configuration.

From Fig. 3.8 we can write

$$V_{out} = H_A(j\omega) \cdot V_d \tag{3.1}$$

$$V_f = H_F(j\omega) \cdot V_{out} \tag{3.2}$$

and

$$V_d = V_{in} + V_f \tag{3.3}$$

By combining the transfer functions of the amplification stage $H_A(\omega)$ with the feedback stage $H_F(\omega)$ to the closed-loop transfer function, can be established the mathematical condition for a circuit to oscillate:

$$\frac{V_{out}}{V_{in}} = H_{CL}(j\omega) = \frac{H_A(j\omega)}{1-H_F(j\omega)H_A(j\omega)} \tag{3.4}$$

Since there is no input to an oscillator, V_{in} = 0, to obtain a nonzero output voltage, V_{out}, the denominator in (3.4) has to be zero. This requirement leads to the Barkhausen criterion, which is also known as the *loop gain* equation:

$$1 - H_F(j\omega)H_A(j\omega) = 0 \tag{3.5}$$

or

$$H_F(j\omega)H_A(j\omega) = 1 \tag{3.6}$$

Equation (3.6) expresses the fact that for oscillations to occur the loop gain must be unity, satisfying the Barkhausen criterion.

With $H_A(j\omega) = H_{Ao}$ and

$$H_F(j\omega) = H_{F_r}(\omega) + jH_{F_i}(\omega) \tag{3.7}$$

where $H_{F_r}(\omega)$ and $H_{F_i}(\omega)$ are the real and imaginary parts of $H_F(j\omega)$, we can express (3.6) in the form

$$H_{F_r}(\omega)H_{Ao} + jH_{F_i}(\omega)H_{Ao} = 1 \tag{3.8}$$

Equating the real and imaginary parts on both sides of the equation is obtained

$$H_{F_r}(\omega)H_{Ao} = 1 \Rightarrow H_{Ao} = \frac{1}{H_{F_r}(\omega)} \tag{3.9}$$

and

$$H_{F_i}(\omega)H_{Ao} = 0 \Rightarrow H_{F_i}(\omega) = 0 \tag{3.10}$$

for $H_{Ao} \neq 0$. The conditions in (3.9) and (3.10) are known as the Barkhausen criteria in rectangular form for $H_A(j\omega) = H_{Ao}$.

The condition (3.9) is known as the gain condition, and (3.10) as the frequency of oscillation condition. The frequency of oscillation condition predicts the frequency at which the phase shift around the closed loop is 0° or a multiple of 360°.

The equation (3.6) can also be expressed in polar form as

$$H_F(j\omega)H_A(j\omega) = |H_F(j\omega)H_A(j\omega)|\,\angle H_F(j\omega)H_A(j\omega) = 1$$

Accordingly, results

$$|H_F(j\omega)H_A(j\omega)| = 1 \tag{3.11}$$

and

$$\angle H_F(j\omega)H_A(j\omega) = \pm n360° \tag{3.12}$$

where n = 0, 1, 2, 3, … In equation (3.12) is established the fact that the signal must travel through the closed loop with a phase shift of 0° or a multiple of 360°. For $H_A(j\omega) = H_{Ao}$, then $\angle H_F(j\omega)H_{Ao}$ is the angle of $H_F(j\omega)$, and the equation (3.12) is equivalent to saying that $H_{F_i}(j\omega) = 0$, according to (3.10). As well, for $H_A(j\omega) = H_{Ao}$ and with $H_{F_i}(j\omega) = 0$, equation (3.11) is reduced to (3.9). The terms in (3.11) and (3.12) are the Barkhausen criteria in polar form [23].

In this work were considered two types of current-controlled oscillators to implement in order to realize the project. The oscillator 1 and oscillator 2, with the differences between both to be described below.

3.3.1. Oscillator 1 (CCO 1)

The oscillator presented here is a ring oscillator composed by an odd number of inverters, in this case three inverters, shown in Fig. 3.9. This configuration of oscillator is best analysed in terms of the time/propagation delay that the signal experiences as it goes through the ring inverters. Considering t_p the propagation delay of the inverter, the frequency of oscillation is given by

$$f_o = \frac{1}{2nt_p} \tag{3.13}$$

where *n* is the number of gates.

The data provided by manufacturers of inverters in relation to the propagation delay is as a function or the device load capacitance. Although, the resultant frequency of oscillation can vary substantially from the expected frequency resultant in (3.13).

It is difficult to properly control the frequency of oscillation, since it is controlled by the propagation delay. The propagation delay is affected by many factors, including the variation in

output capacitance from unit to unit. The solution for better control of the frequency of oscillation involves adding external elements [23].

Despite high signal distortion and noise, ring oscillators are used in many high speed digital circuits due to an ease of integration, small chip area, high oscillation frequencies and wide tuning ranges [24].

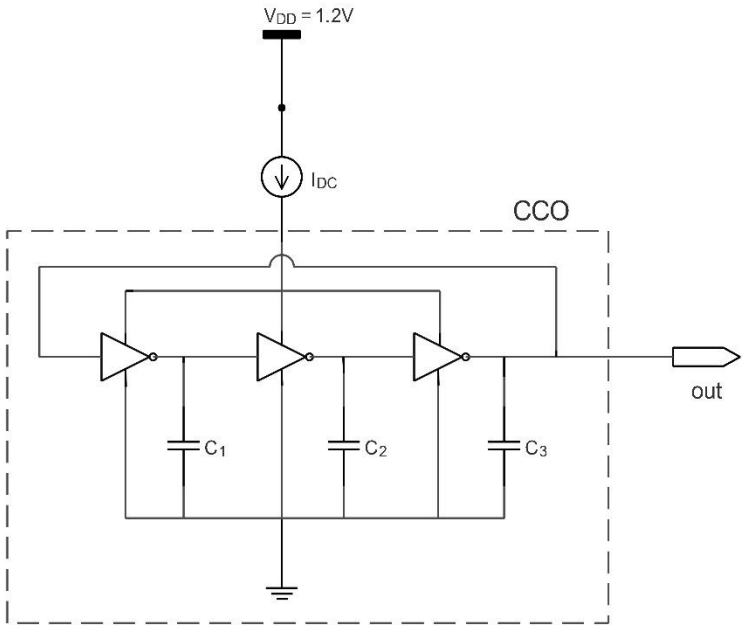

Figure 3.9 – Circuit schematic of oscillator 1 (CCO 1) based on a ring-oscillator configuration.

3.3.2. Oscillator 2 (CCO 2)

The oscillator covered in this section is the current-starved voltage controlled ring oscillator, and is similar to the oscillator 1, but is composed by more transistors.

CMOS voltage/current controlled oscillator (VCO/CCO) are critical building blocks in phased-locked loops (PLLs), and they are mainly responsible for having the highest fraction of the overall power consumption and occupied area of the system. Furthermore, a VCO/CCO constitutes one of the most important components in many RF transceivers and are commonly associated with signal processing tasks like frequency (channel) selection and signal generation.

VCOs/CCOs occupy an important role in communication systems, giving periodic signals required for timing in digital circuits and frequency translation in RF circuits. The output frequency of a VCO/CCO is a function of a control input, normally a voltage. In an ideal voltage controlled oscillator the output frequency is a linear function of its control voltage.

A current starved VCO/CCO operates similarly to the ring oscillator. The transistors M_4, M_5, M_8, M_9, M_{12} and M_{13} operate as inverters, while transistors M_3, M_6, M_7, M_{10}, M_{11} and M_{14} operate as current sources, as can be seen in Fig.3.10. Those current source transistors limit the

current available to the inverter transistors. In other words, the inverter is starved for current. The drain currents of MOSFETs M_1 and M_2 are the same and are set by the input control voltage. The currents in transistors M_1 and M_2 are mirrored in each inverter/current source stage [46][47].

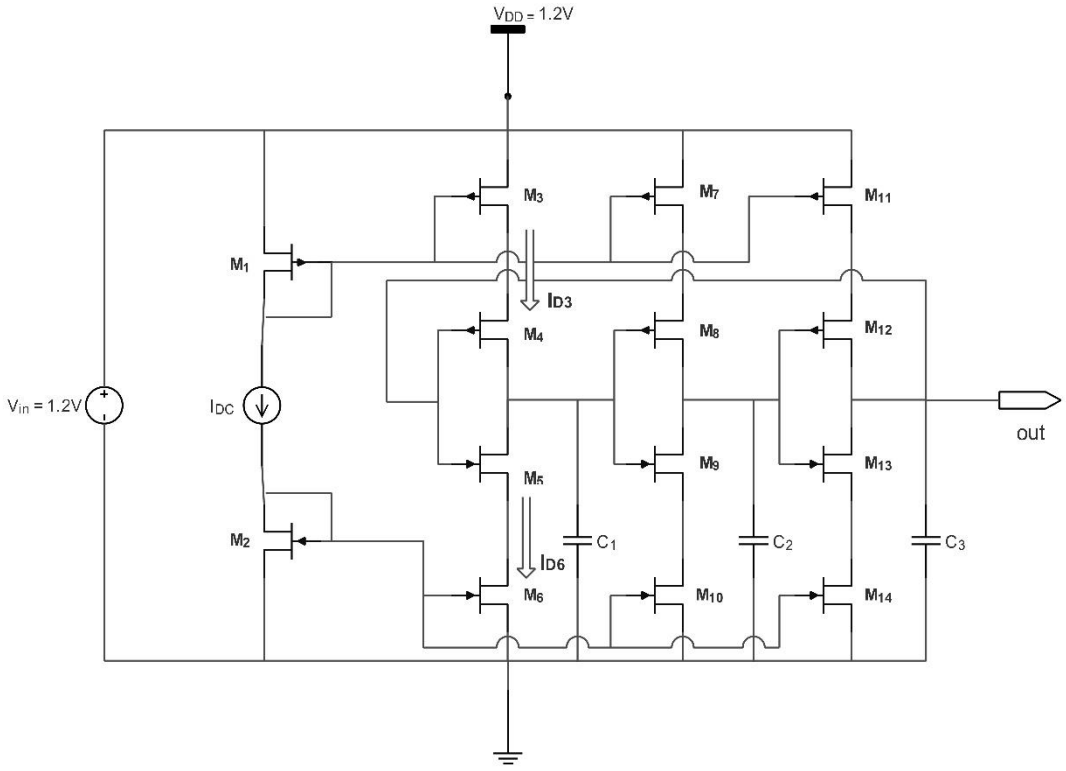

Figure 3.10 – Circuit schematic of oscillator 2 (CCO 2).

This oscillator has three stages, and the centre drain current is given as:

$$I_{D_{Centre}} = N \times V_{DD} \times C_{tot} \times F_{cen} \tag{3.14}$$

where N is the number of stages of the inverter. The sizes of transistors M_1 and M_2 are determined as:

$$I_{D_{Centre}} = \frac{\beta(V_{gs}-V_{thn})^2}{2} \tag{3.15}$$

where, $\beta = \frac{K_p \cdot W}{L}$.

The oscillation frequency of the current-starved VCO/CCO for N stages is:

$$F_{osc} = \frac{1}{N} \cdot T_D = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}} \tag{3.16}$$

T_D is the time delay above equation gives the centre frequency of the VCO/CCO when $I_D = I_{D_{Centre}}$. Neglecting sub threshold currents, the oscillation of the VCO/CCO is interrupted when $V_{in_{VCO}} < V_{thn}$. Therefore, $V_{min} = V_{thn}$ and $F_{min} = 0$. The maximum VCO/CCO oscillation frequency F_{max} is determined detecting I_D when $V_{in_{VCO}} = V_{DD}$. Thus, at the maximum frequency $V_{max} = V_{DD}$ [46][47].

The total capacitance on the drains of transistors M_4 and M_5 for example, is:

$$C_{tot} = C_{out} + C_{in} = C'_{ox}(W_4L_4 + W_5L_5) + \frac{3}{2}C'_{ox}(W_4L_4 + W_5L_5) = \\ = \frac{5}{2}C'_{ox}(W_4L_4 + W_5L_5) \quad (3.17)$$

where C_{out} and C_{in} are the output and input capacitances respectively.

To charge C_{tot} form zero to V_{SP} with the constant current I_{D3} is taken a certain amount of time that is expressed by:

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D3}} \quad (3.18)$$

where V_{SP} is switching point of the inverter.

And the time C_{tot} takes to discharge from V_{DD} to V_{SP} is expressed by:

$$t_2 = C_{tot} \cdot \frac{V_{DD} - V_{SP}}{I_{D6}} \quad (3.19)$$

Setting $I_{D3} = I_{D6} = I_D$ (which will be designated by $I_{D_{centre}}$ when $V_{in_{VCO}} = \frac{V_{DD}}{2}$), then the sum of t_1 and t_2 will be:

$$t_1 + t_2 = \frac{C_{tot} \cdot V_{DD}}{I_D} \quad (3.20)$$

3.4. Transconductance Stage (*gm*)

The transconductance stage (*gm*) is mainly built using a differential-pair with active loads. A differential pair is a basic circuit in electronics. It can be used as an amplifier with differential

input, constituting the input stage of the operational amplifiers, which determines most of the non-ideal characteristics of these amplifiers. In some cases, a differential pair with active loads behaves itself as a moderate gain operational transconductance amplifier (OTA).

Differential pairs and differential transconductors, in general can be used in analog continuos-time filters (Gm-C filters), RC-active filters analog multipliers and in many other circuits derived from it, such as modulators and phase detectors. The differential pair with active loads is the fundamental constituent of analog and mixed-signal integrated circuits [35].

3.5. Digital-to-Analog Converter

The conversion between analog and digital signals is one of the most important functions in signal processing. There are areas where signal processing is done on analog signals and areas where the signal processing is done on digital signals. Hence, there is a need to convert analog-to-digital and digital-to-analog between the two types of signals. Thus, these converters, respectively ADCs and DACs, play an important role in any signal-processing system [33].

The different approaches to convert a digital signal to an analog signal include speed, chip area, power efficiency and achievable accuracy. Wherein, for a given and specific application, it is necessary to know which converter algorithms or architectures to choose.

DACs are sampled data systems, thus they require the use of circuit techniques that can deal with discrete-time analog signals. The circuits are frequently divided into voltage-mode or current-mode circuits, according the analog signals are voltages or currents. In CMOS, for voltage-mode circuits is normally used the switched-capacitor (SC) technique while for current-mode circuits is used the switched-current (SI) technique [31].

The DAC input is a digital information made of parallel binary signals generated from a digital signal-processing system. These parallel binary signals go through conversion process to a similar analog signal. In the output, the analog signal can be amplified and/or filtered before being applied to an analog signal-processing system. The input and output in most DAC's are voltage signals, although, they can be other physical quantities, such as current or charge [32][33].

In other words**,** DAC is a digital-to-analog converter, that has a function to convert digital data into an analog signal, that can be a current, a voltage or simply an electric charge. That device is responsible for converting an abstract finite-precision number into a physical quantity/concrete sequence of impulses, which is subsequently processed by a reconstruction filter.

There are many different DAC architectures, that include Nyquist-Rate DAC, Binary Weighted DAC (Current-Steering DAC, R-2R Ladder DAC, Charge Redistribution DAC), Thermometer Coded DAC, Encoded DAC, Hybrid DAC, Low-Speed DAC (Algorithmic DAC,

Switched-Current Algorithmic DAC), Pipelined DAC, Oversampling DAC (M-bit DAC), and Delta-Sigma DAC.

The block diagram presented in Fig. 3.11, describes a DAC with voltage output. It consists of a reference voltage V_{REF}, and digital information of *N*-bits ($b_0, b_1, \dots, b_{N-1}$) where b_0 is the *most significant bit* (MSB), and b_{N-1} is the *least significant bit* (LSB). The voltage output V_{out} can be mentioned as

$$V_{out} = KV_{REF}D \tag{3.21}$$

where *K* is a scaling factor and the digital information *D* is given as

$$D = \frac{b_0}{2^1} + \frac{b_1}{2^2} + \cdots + \frac{b_{N-1}}{2^N} \tag{3.22}$$

where *N* is the total number of bits of the digital word and b_{i-1} is the *i*th-bit coefficient and is 0 or 1. Thence, the output of a DAC can be expressed matching eq. (3.21) and (3.22) to obtain

$$V_{out} = KV_{REF} = \left[\frac{b_0}{2^1} + \frac{b_1}{2^2} + \cdots + \frac{b_{N-1}}{2^N}\right] \tag{3.23}$$

or

$$V_{out} = KV_{REF} = [b_0 2^{-1} + b_1 2^{-2} + \cdots + b_{N-1} 2^{-N}] \tag{3.24}$$

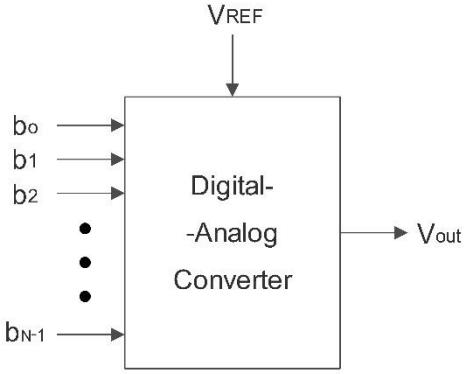

Figure 3.11 – Digital-analog converter (DAC) in applications of signal-processing.

In order to understand the design of DAC, it is important his characterization. There are two important performance characteristics of digital-analog converters, namely static and dynamic properties. The DAC's resolution is given by the number of bits in the applied digital input information. Its resolution is expressed as *N*-bits, where *N* is the number of bits. In Fig. 3.12, is

presented the output characteristic of an ideal 3-bit DAC ($N = 3$). For each of eight possible digital words matches its own unique analog output voltage, whose levels are separated by an *LSB*, and ist value can be expressed as

$$LSB = \frac{V_{REF}}{2^N} \tag{3.25}$$

and as the digital word increases by 1-bit, the output of the ideal DAC must jump by 1 *LSB* [33].

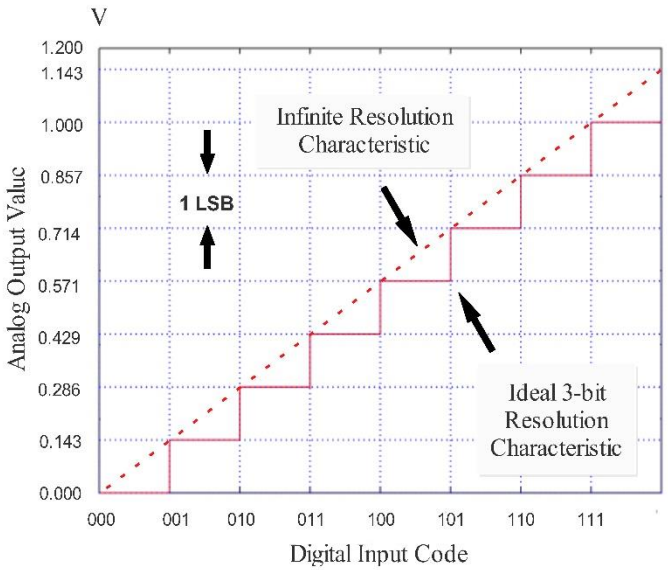

Figure 3.12 – Ideal characteristics of input-output for 3-bit DAC.

As the resolution of the DAC is not infinite, the maximum analog output voltage is different from V_{REF}. The *full-scale* (FS) value of the DAC describes this result. The difference between the analog output for the largest digital word (111) and the analog output for the smallest digital word (000) defines the full-scale value. Usually, the DAC's full scale can be established as

$$\text{Full Scale (FS)} = V_{REF} - LSB = V_{REF}\left(1 - \frac{1}{2^N}\right) \tag{3.26}$$

and the *full-scale range* (FSR) is defined as

$$FSR = \lim_{N\to\infty} FS = V_{REF} \tag{3.27}$$

where *FS* is the analog output voltage for the largest digital word (111 in this case) [33].

An important aspect about DAC relates to certain types of errors. There should be a unique analog output signal for each digital word, and any gap from ideal *n*-bits resolution characteristic belongs to static-conversion errors. These type of errors include, gain errors, offset errors, differential nonlinearity, integral nonlinearity, and monotonicity. Wherein *gain error* is the difference between the actual finite resolution and an infinite resolution characteristic measured at the rightmost vertical jump. *Offset error* is a constant difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured at any vertical jump. *Differential nonlinearity* ia a measure of the separation between adjacent levels measured at each vertical jump. *Integral nonlinearity* is the maximum difference between the actual finite resolution characteristic and the ideal finite resolution characteristic measured vertically. And *monotonicity* means that as the digital input to the converter increases over its full-scale range, the analog output never exhibits a decrease between one conversion step and the next [33].

3.5.1. The 6 bit IDAC

The DAC presented in this work is a 6 bit IDAC shown in Fig. 3.13

The architecture of this IDAC is based on a current-steering approach and it consists of a current replication network which generates weighted currents in the form of independent current sources, a current switching network controlled by the binary bits, and a resistance R_1 responsible for converting the current to voltage.

In other words, this IDAC comprises six input inverters, each one connected to its unit device circuit. The number of unit device circuits corresponds to the number of bits of this DAC, wherein each unit device circuit has a certain *width* value in all its transistors. Starting from the lower unit device circuit (the least significant weight) to the upper unit device circuit (the most significant weight), the *width* value grows exponentially with a power of 2 between each unit device circuit. The DAC number-of-bits presented in this work is determined by the resolution (*N*) of bits, with $N = 6$, and satisfying the equation 2^N = nº of levels, results in $2^6 = 64$ levels (LSBs). This 6 bit IDAC for a certain digital input code corresponds to a given analog output voltage.

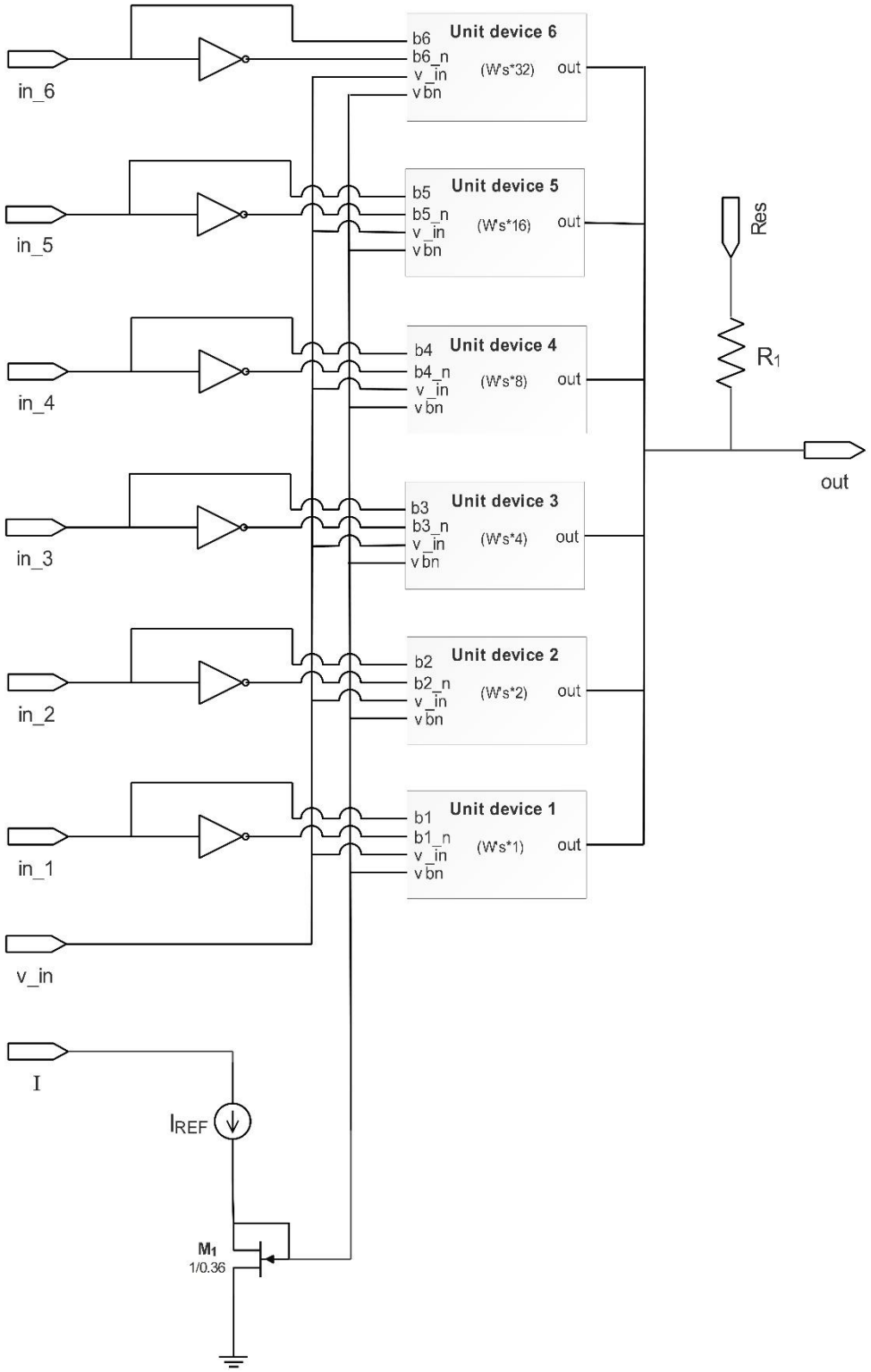

Figure 3.13 – Simplifier circuit schematic of 6 bit IDAC.

Each of the unit device circuit has an NMOS cascode current-source, whose transistors are sized up according to the corresponding bit weight and are biased by the same bias voltages. This type of current source was preferred in detriment to the simple current source, because, cascode current source presents a higher output impedance that makes the IDAC more accurate. Requires

switches, mainly built by NMOS and PMOS devices, have their sizes are scaled up according to the bit values as well. In this case, partitioning is applied to the weighted sources and each weighted current source is made of a number of LSB devices connected in parallel, where the LSB device becomes the unit device. By partitioning the weighted devices in units so that the MSB consists of 2^{N-1} unit devices, as can be seen in a theortical example presented in Fig.3.14 [38].

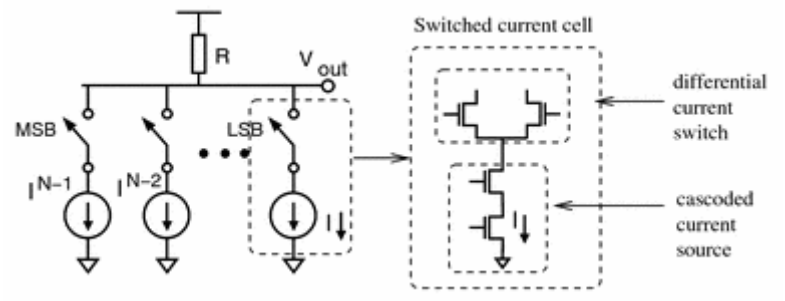

Figure 3.14 – Simple-binary weighted current steering DAC and its implementation with transistors [38].

This type of implementation is compact and very simple, presenting high rates of conversion, but is limited by the process limitations, by the maximum switching speed switching the current, and by the steepness of the of the data waveforms carrying the bits. Also, there are some disadvantages of this type of circuit realization that results in a limitation of its performance, mainly because of its simplicity and low power consumption.

One of these problems is associated with the weighted impact of switching problems, also named MSB/LSB glitches. This condition is verified because of imperfect synchronization of the data waveforms that control the current switches. As an example, in a 8 bit binary weighted DAC at the midscale transition 01111111 → 10000000 the MSB current source turns on and all the remaining bits turn off. Also, if the MSB source turns on a bit earlier than the remaining sources turn off, then for a time interval the code 11111111 will appear before the 10000000. And this momentary voltage spike, that is the principal carry glitch in the normal operation of the DAC, is responsible for creating a harmonic distortion.

As a solution for these types of glitches of CS DAC's, have been created and implemented the famous *de-glitching circuits* [38]. However, in the particular case of this work, since the operating speed is not an issue and since the required resolution is quite low (N = 6 bits), none of the previously referred problems represent a critical problem for the temperature sensor system.

3.6. Electro-Thermal Filter (ETF)

The accuracy of timing signals plays an important role in operation and performance of electronic systems. The quartz crystal oscillators were used for several years to generate those signals, which have the disadvantage of inability to use in microchips. Many attempts have been realized to the achievement of integrated frequency references, giving rise to different types of silicon-based frequency references, including MEMS (Micro Electro Mechanical System) resonator with a silicon chip, integrated resistors, capacitors and inductors.

Electrothermal filters represents an alternative to the realization of integrated frequency references, relying on the thermal properties of bulk silicon leveraged by electrothermal structures, instead of relying on the accuracy of on-chip electrical components. Those electrothermal structures are controlled by thermal-diffusivity, a physical parameter that is a measure of the rate at which heat diffuses through a silicon substrate [36].

The physical domains of electricity, mechanics, chemistry, electromagnetism, and thermicity, can be used in order to produce, process and transfer energy, where the electrical, mechanical and electromagnetic domains historically has obtained preference to generate stable on-chip frequency references, and was given less attention to the *thermal-domain* properties of silicon. These were investigated with more attention from the seventies, referring in particular to the transport of thermal signals in microelectronic structures. The interactions between electrical and thermal-domain signals can be used to produce large time constants in silicon integrated circuits, as demonstrated by Gray and Hamilton in 1971.

Thermal-diffusivity can be availed in a standard CMOS process, because through standard CMOS compatible structures called the ETFs, can be simulated the behaviour of thermal diffusivity of silicon, where ETF is a low-pass structure with phase response determined by *D* and by geometry.

Some experiments with thermal-diffusivity-based (TD) temperature sensors proved that EFT tolerances are about 0.1 %, determinated by the purity of the silicon substrate and by the accuracy of the lithography used in the IC technology. This lithographic accuracy improves in scaled processes, with smaller feature sizes, implying that the ETF benefits from Moore's law.

Along the design and size process of an electro-thermal frequency reference, is necessary to take into account the trade-offs between accuracy, output frequency and jitter performance. The thermal delay is set by ETF's geometry, wherein the smaller the geometry, the smaller the delay and therefore the higher the output frequency of the reference can be. In contrast, the accuracy of the output frequency is determined by the accuracy of an ETF's phase shift. And where the increased ETF's dimensions improve its intrinsic accuracy, but reducing its output signal, and increasing the effect of ETF's wideband thermal noise on the frequency-locked loop's jitter [36].

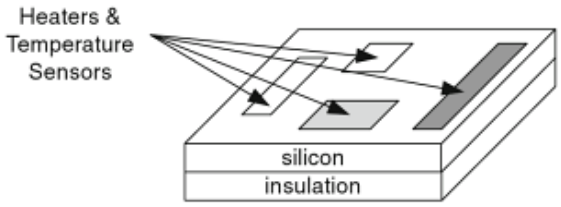

Figure 3.15 – Diffusion of temperature sensors and micro heaters on a silicon substrate [36].

After some research, it was found that in the microstrucures in which integrated heaters were fabricated close to integrated thermal sensors and within a silicon substrate (Fig. 3.15), the heat generated in the heater diffuses through the substrate and is sensed by the temperature sensor after a certain *thermal delay*. This delay is associated with the substrate's thermal inertia, and involves the transfer of heat within a defined geometry, fabricated in a silicon substrate, where this acts as the heat transferring medium. In the silicon slab the diffusion heater (ex: resistor) is implemented closly to a relative temperature sensor (ex: thermopile), where the distance *s* is a few tens of microns (Fig. 3.16).

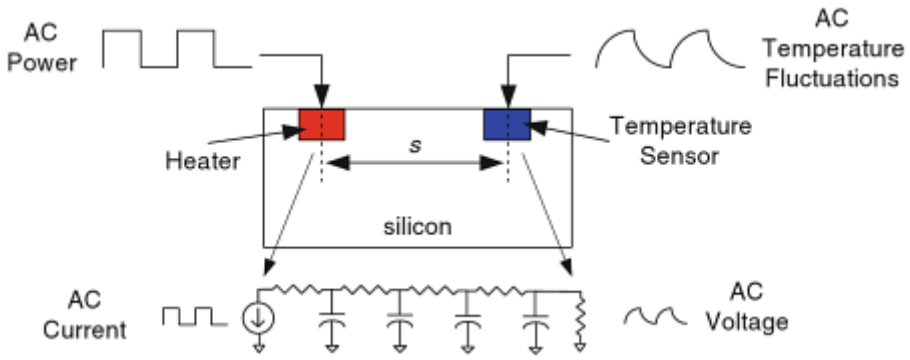

Figure 3.16 – Side view of a silicon slab [36].

Through the substrate is diffused the heat generated in the heather, resulting in a local temperature change, mediated by phonons, involving mechanical vibration within the silicon atoms of the lattice. Where phonons are a combined excitation in a periodic, elastic disposition of atoms/molecules in condensed substance (e.g.: solids/liquids), and it represents an excited state in the quantum mechanical quantization of the modes of vibrations of elastic structures of interacting particles, commonly projected as quasiparticle [37].

In other words, phonons are the discrete amounts of quanta energy that the collective vibrational modes can accept based on the behaviour of vibrational energy in periodic solids. And considering a solid to be a periodic array of mass points, there are constraints on both the minimum and maximum wavelength associated with a vibrational mode, as can be observed in the Fig. 3.17.

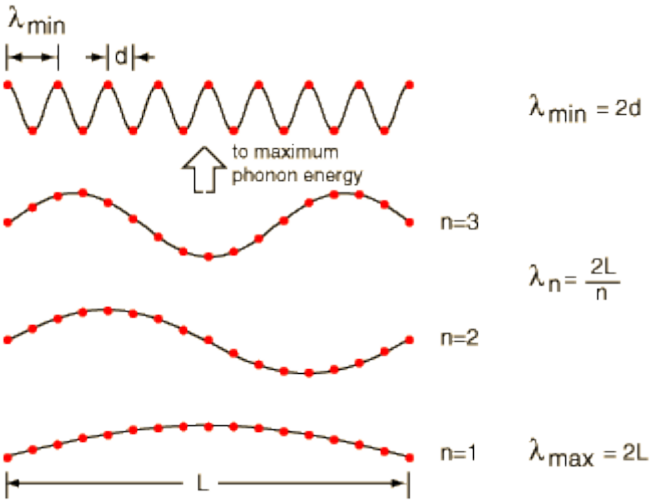

Figure 3.17 -Vibrational mode of phonons.

where the energy of the phonon is given by the following expression:

$$E = hv = \frac{hV_s}{\lambda} = \frac{hV_s n}{2L} \tag{3.28}$$

with V_s representing the speed of sound in the solid.

The temperature dependent parameter *D*, that is the thermal-diffusivity of silicon, determines the rate at which heat diffuses through the substrate. The temperature has the effect of expansion or contraction on the silicon lattice, affecting the mechanical vibration of the crystalline silicon atoms. Therefore, it is concluded that the thermal delay resulted from the thermal diffusivity of silicon is a function of temperature.

In Fig. 3.16, when the AC power is dissipated in the silicon slab, temperature fluctuations are originated at the temperature sensor, which are translated back into an AC electrical signal, with the phase of this signal being delayed relatively to the power of heater. Where this delay is a function of *s* and *D*. Thus, this type of composition resembles a low-pass filter and is accordingly called an ETF, with a defined phase versus frequency characteristic, as the electrical filter, with possibilities to be employed in any integrated circuit fabrication process [36].

Other researches led to the use of the thermoelectric effect, based on the direct conversion of temperature difference to electric voltage, in order to perform on-chip temperature sensors in the form of thermocouples, giving rise to a thermal oscillator.

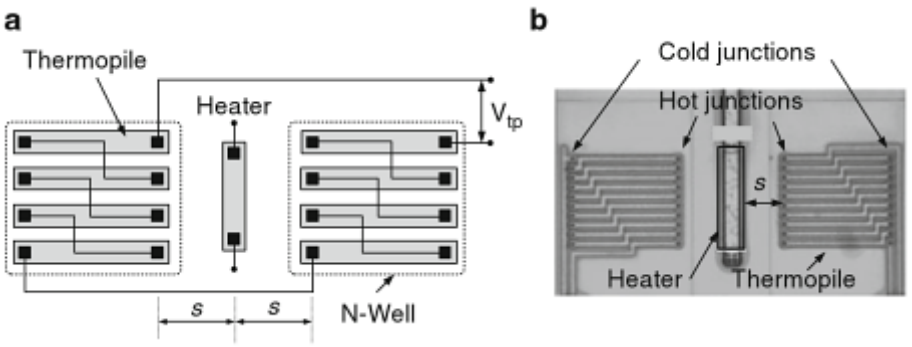

Figure 3.18 – Simplified schematic layout (a), and photomicrograph (b) of the optimized CMOS ETF [50].

In Fig.3.18 can be observed the simplified schematic layout and photomicrograph of the optimized electro-thermal filter designed in a 0.7 um CMOS process with bar-shaped heater and rectangular thermopile, and its streamlined cross section with different layers in Fig.3.19.

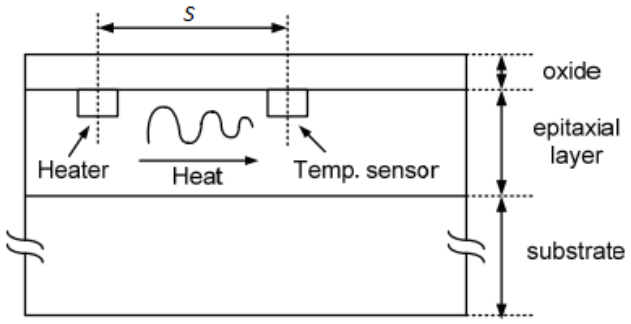

Fig. 3.19 – A streamlined cross section of an ETF in standard CMOS [49].

Chapter

Design Methodology and Sizing

4

In the present chapter is presented the design methodology and sizing process of the TDT sensor's transistors. The circuit is divided into digital and analog parts, where the digital part has a much simplier sizing process. In order to size the transistors of the analog part, were used various formulas to find the best width to length ratio.

4.1. Digital Part

In the digital part of the TDT sensor system, the transistor dimensions considered were the same for all the digital blocks (built from the standard INV, NAND and NOR logic gates and switches), with $W = 2\ \mu$m and $L = 0.12\ \mu\text{m} = L_{min}$ for the NMOS transistors, and $W = 8\ \mu$m and $L = 0.12\ \mu\text{m} = L_{min}$ for the PMOS devices, Hence, the W's ratio between PMOS and NMOS transistors was 4/1, being a good ratio for that transistors operate as switches and, on the other hand, to guarantee symmetrical rising and falling times in the digital logic cells.

4.2. Analog Circuitry

In the analog part of the TDT sensor system the transistor dimensions have been optimized taking into account the different circuit topologies employed.

4.2.1. Oscillator 1 (CCO 1)

Since the oscillator is constituted basically by digital CMOS inverters, the size of transistors described in the subchapter 4.1 relatively to digital part have been used.
Regarding the loading capacitors, and inn order to have at the output a frequency span between 200 and 250 MHz, and an amplitude output voltage of about 800 mV, the three capacitors were sized equally with 300 fF.

It worth mentioning that the output frequency was set between 200 and 250 MHz to meet the initial specifications of the TDT Sensor circuit. And the amplitude output voltage was set around 800 mV in order to have enough amplitude levels to properly drive the 6 bit counter.

4.2.2. Oscillator 2 (CCO 2)

In this type of oscillator (Fig.4.1), are going through sizing process the three capacitors C_1, C_2 and C_3, the inverter transistors M_4, M_5, M_8, M_9, M_{12} and M_{13}, the current source transistors M_3, M_6, M_7, M_{10}, M_{11} and M_{14}, and the current mirror transistors M_1 and M_2.

Regarding to the inverter transistors, the same sizing used in oscillator 1 has been adopted, namely with $L = L_{min}$ in all transistors, with $W = 4\ \mu m$ in all PMOS transistors, and with $W = 1\ \mu m$ in all NMOS devices, satisfying the 4/1 ratio between PMOS and NMOS transistors.

About the transistors which implement the basic NMOS and PMOS current-sources, transistors, $L = 3L_{min}$ in order to avoid channel modulation effects, and short channel effects. And the W sizing between PMOS and NMOS transistors is the same as in the inverter transistors. The same strategy has been followed in the sizing process of the current mirror transistors.

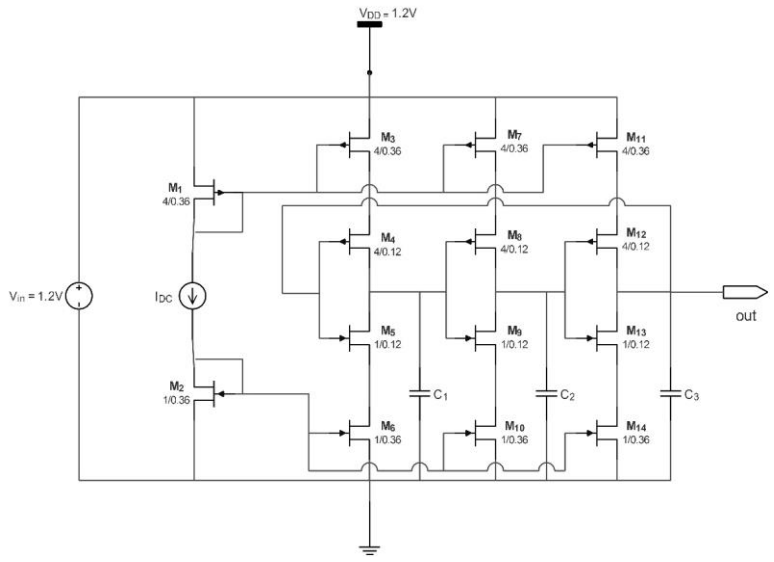

Figure 4.1 – Transistor sizing of oscillator 2.

4.2.3. Transconductance Stage (*gm*)

In order to obtain the size parameters of transistors of the present circuit of Fig.4.2, is used the following equation:

$$I_D = \frac{1}{2} K_{n,p} \frac{W}{L} (V_{GS} - V_{TN,TP})^2 = \frac{1}{2} K_{n,p} \frac{W}{L} {V_{DSsat}}^2 \tag{4.1}$$

where

$$\frac{W}{L} = \frac{I_D}{\frac{K_{n,p}}{2} \cdot {V_{DSsat}}^2} = \frac{2I_D}{K_{n,p} \cdot {V_{DSsat}}^2} \tag{4.2}$$

with

$$K_n = \mu_n \cdot C_{ox} \cong 500\mu A \cdot V^{-2} \tag{4.3}$$

and

$$K_p = \mu_p \cdot C_{ox} \cong 150\mu A \cdot V^{-2} \tag{4.4}$$

The transconductance *gm* is expressed by:

$$gm = \sqrt{2 \cdot K_{n,p} \frac{W}{L} I_D} = K_{n,p} \cdot \frac{W}{L} \cdot V_{dsat} = \frac{2 \cdot I_D}{V_{dsat}} \tag{4.5}$$

With a current I_D = 15 uA it was obtained the following sizing for transistors M_1 and M_2:

$$\frac{W}{L} = \frac{2I_D}{K_n \cdot {V_{DSsat}}^2} = \frac{2 \cdot (15E-6)}{(500E-6) \cdot 0.05^2} = 24 \tag{4.6}$$

as the transistors M_1 and M_2 built the differential pair's tail current source, their transistor length is as much as possible, with $L = 0.5\ um$ and, therefore, the corresponding transistor width yields $W = 12\ um$.

Since transistors M_3, M_4, M_5 and M_6 are drawing a current of $\frac{I_D}{2} = 7.5\ uA$, they can be sized accordingly to:

$$\frac{W}{L} = \frac{2I_D}{K_n \cdot {V_{DSsat}}^2} = \frac{2 \cdot (7.5E-6)}{(500E-6) \cdot 0.05^2} = 12 \tag{4.7}$$

with transistor length as much as possible for a normal transistor, setting $L = 0.36\ um$, resulting in a transistor width of $W = 4.32\ um$.

For transistors M_7 and M_8, the sizing process is similar and relatively straightforward, compared to previous transistors, yielding:

$$\frac{W}{L} = \frac{2I_D}{K_p \cdot V_{DSsat}{}^2} = \frac{2 \cdot (7.5E-6)}{(150E-6) \cdot 0.05^2} = 40 \tag{4.8}$$

resulting in $W = 14.4\ um$, because transistor length is also $L = 0.36\ um$, for the same reasons described before.

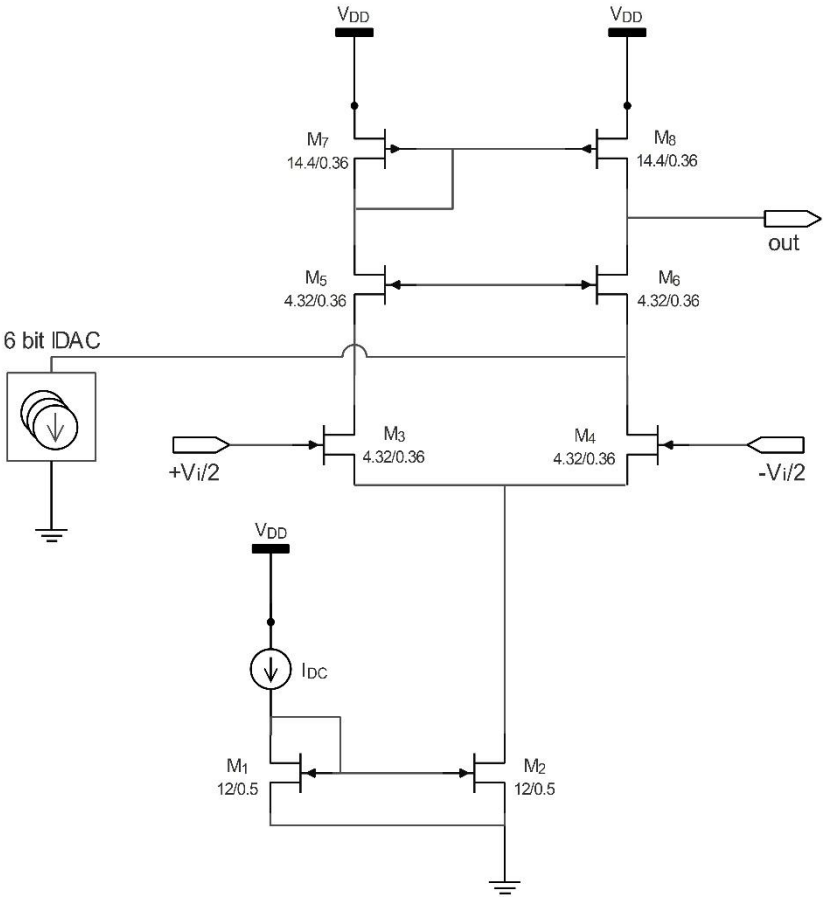

Figure 4.2 – Circuit schematic of differential pair and 6 bit IDAC, constituting gm stage.

The size of all transistors can be seen in the Tab.4.2 presented below.

Table 4.1: Size of all transistors used in the transconductance stage.

Transistor	$L(\mu m)$	$W(\mu m)$
M_1	0.5	12
M_2	0.5	12
M_3	0.36	4.32
M_4	0.36	4.32
M_5	0.36	4.32
M_6	0.36	4.32
M_7	0.36	14.4
M_8	0.36	14.4

4.2.4. Electro-Thermal Filter (ETF)

The ETF used in this project is constituted by five resistances and five capacitors, as represented in Fig.4.3. The DC voltage source V_{pulse} was used to tune its amplitude and phase shift variation between the input and output waves. The operating range of this ETF is 45º, varying from 0º to 45º. Hence, all the elements need to be sized in order to cover all this range, with $R_{1,2,3,4} = 0\ \Omega$, R_{out} =500 kΩ, $C_{1,2,3,4} = 3$ pF for a phase shift of 0º, and with $R_{1,2,3,4} = 30.5\ k\Omega$, R_{out} =500 kΩ, $C_{1,2,3,4} = 3$ pF for a phase shift of 45º, always with $V_{pulse} = 1.17$ MHz of frequency. Please keep in mind that this circuit is simply an electrical model of an Electro-Thermal system that has been referred before. In practice this circuit has been modelled solely to allow complete transient electrical simulations of the complete temperature sensor system.

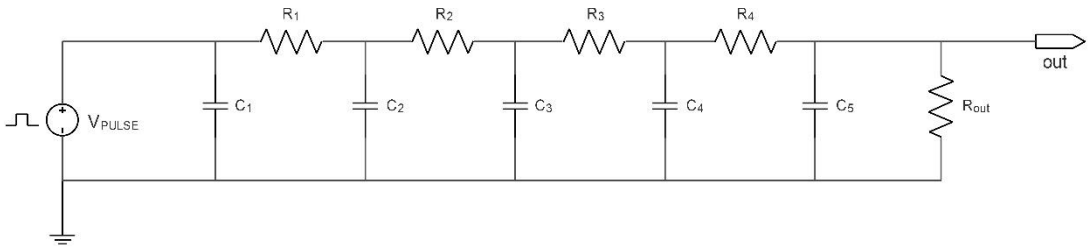

Figure 4.3 – Electro-Thermal Filter circuit.

4.2.5. The 6 bit IDAC

Each unit device circuit is composed by four transistors (2 PMOS and 2 NMOS). This circuit is shown in Fig.4.4, where the transistors M_1 and M_2 implement the cascode current source, transistor M_3 is the switch from the left side, and transistor M_4 is the switch that adds the current corresponding to the weighted associated by the given bit driving the switch.

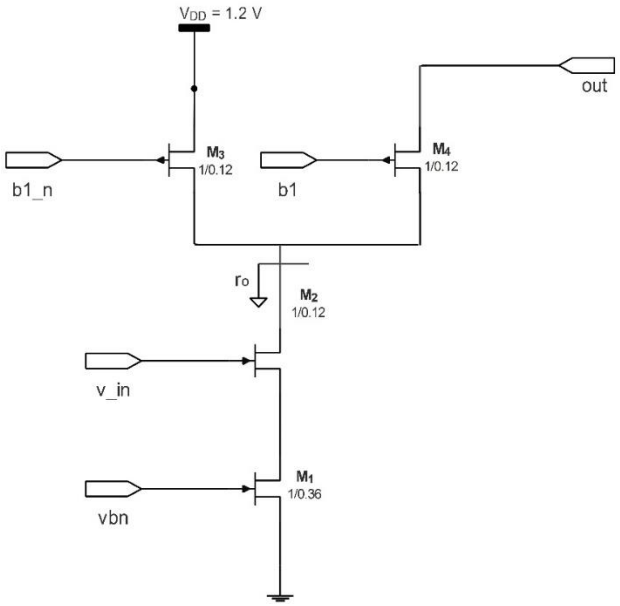

Figure 4.4 – Circuit schematic of 6 bit IDAC´s unit device.

In the first unity circuit the transistor dimensions are presented in Fig.4.4. As the transistors M_1 and M_2 realize the cascode current source, is it important that at least one of them has a relatively large L, $L = 3L_{min} = 0.36\,\mu$m in this case, in order to avoid channel modulation effects, and short channel effects. Also, the output resistance is equal to $r_o = r_{ds1}\left(\frac{gm_2}{gds_2}\right)$ and $r_{ds} \propto L$, and as we want to have a large r_o to avoid the channel effects listed above, L also has to be large enough at least in transistor M_1.

Transistors M_3, and M_4 have $L = L_{min} = 0.12\,\mu$ to function properly as switches. The width of transistors M_1, M_2, M_3 and M_4 of each unit device circuit is equal and a multiple of each anterior unit device circuit in order to have a correct binary count. Starting with $W = 1\,\mu m$ in the first unity current-source (1x I) circuit, and finishing with $W = 32\,\mu m$ in the last current-source circuit (32x I).

In the table 4.2 are presented the final width dimensions of each current-source circuit.

Table 4.2: Width dimensions of the six binary-weighted current-sources.

	Circuits					
Transistor	**Current-Source 1** (μm)	**Current-Source 2** (μm)	**Current-Source 3** (μm)	**Current-Source 4** (μm)	**Current-Source 5** (μm)	**Current-Source 6** (μm)
M_1	1	2	4	8	16	32
M_2	1	2	4	8	16	32
M_3	1	2	4	8	16	32
M_4	1	2	4	8	16	32

Also the resistance R_1, which is located at the output of the unit devices has a value of 2.734 kΩ, resulting from $R_1 = \frac{1.2-0.5}{256 \cdot 10^{-6}} = 2.734\ k\Omega$, and the value of 256 μA results from $2^N \times I_{REF}$, where $N = 6$ and $I_{REF} = 4\ \mu A$. This value of I_{REF} has been adopted because its the value that permits obtaining the maximum amplitude of the stairway-case of the D/A conversion characteristic, ranging from 0.5 V to 1.2 V. For $I_{REF} > 4\ \mu A$, the output goes down beyond 0.5 V and then it is no longer possible to connected the output of this IDAC block to the output of the transconductance stage.

Chapter

5

Simulation Results

In this chapter the simulation results of the constituting blocks and of the final and complete thermal diffusivity temperature sensor system are presented.

5.1. Flip-Flops

Here will be seen the simulation results of the two types of flip-flops used in this TDT Sensor work, the *D* and *JK* flip-flops.

5.1.1. *D* Flip-Flop

In the timing diagram of master-slave negative edge-triggered *D* flip-flop in Fig.5.1, it is observed the output response in relation to the input signal. It can be clearly seen that the output *Q* responds to input *D* on the HIGH-to-LOW transition of the clock pulse, and the *Q'* is the complementary signal.

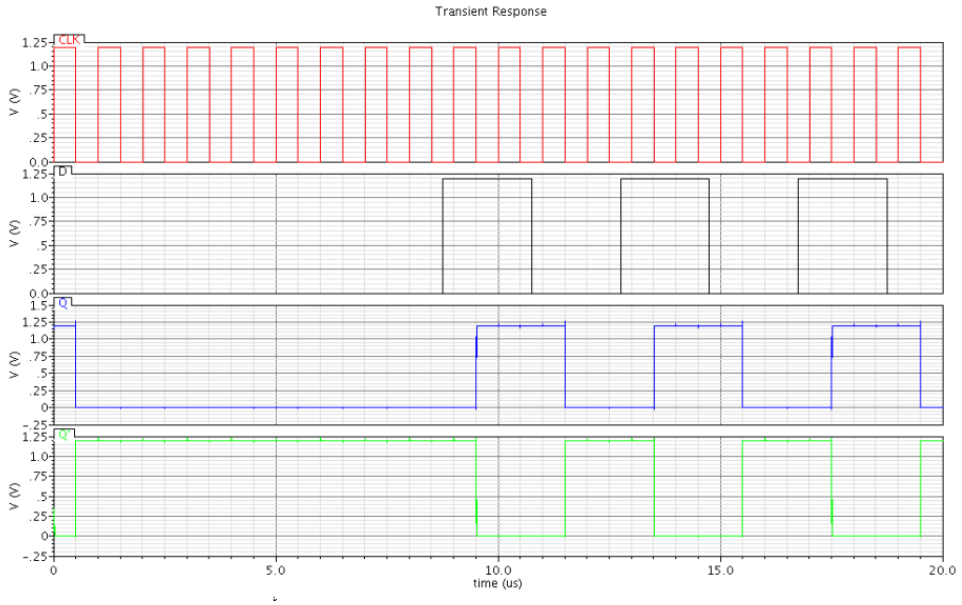

Figure 5.1 – Timing diagram of master-slave negative edge-triggered *D* flip-flop.

5.1.2. *JK* Flip-Flop

In the timing diagram of master-slave negative *JK* flip-flop with *set* and *clear* always *on* in Fig.5.2, is observed the output response in relation to the input signals.

It can be clearly seen that the output *Q* responds to inputs *J* and *K* on the HIGH-to-LOW transition of the clock pulse. At the triggering edge, when *J* is 1 and *K* is 0, output *Q* is 1, if both inputs change their positions to *J* = 0 and *K* = 1, the value of *Q* also turns to 0. And this value of *Q* stays the same if *K* also turn to 0, being *J* = *K* = 0, respecting the condition that output stays the same as it was before. Finally, when *J* = *K* = 1 (both active), the output *Q* is inverted.

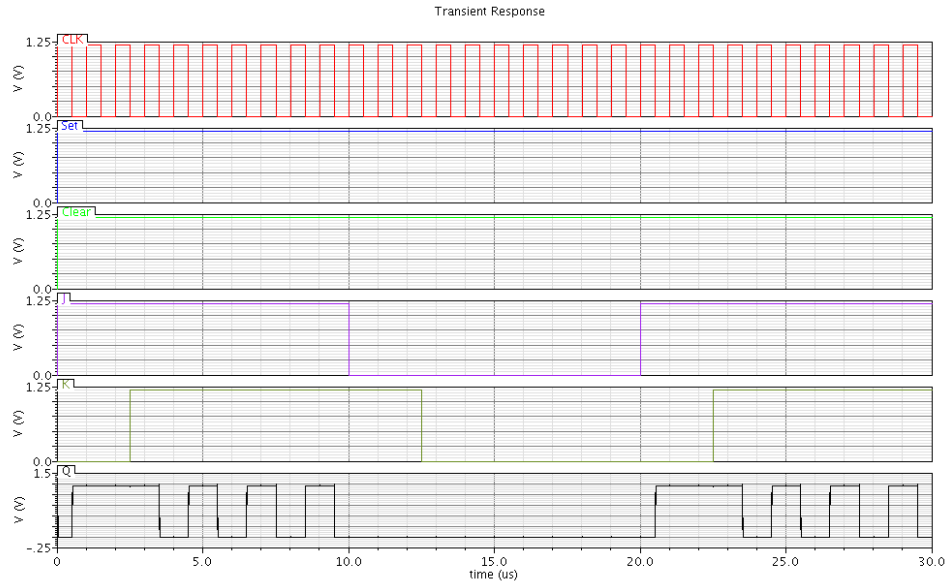

Figure 5.2 – Timing diagram of master-slave negative *JK* flip-flop with *set* and *clear* always *on*.

In the timing diagram of master-slave negative *JK* flip-flop with *set* and *clear* changing, in Fig.5.3, is observed the output response in relation to the input signals, and *set* and *clear* positions.

If *set* is *off* and *clear* is *ON*, the output *Q* stays stable in position 1, whether there is or there is not activity in *JK* flip-flop inputs. When *set* also turns *on*, the activity of *JK* flip-flop returns to normal, as described in Fig.5.2. As *clear* is turned *off*, remaining only *set* active, the output *Q* stays stable in position 0, whether there is or there is not activity in *JK* flip-flop inputs. Finally, when both *set* and *clear* turned *off*, the output *Q* remains stable in position 1, whether there is or there is not activity in *JK* flip-flop inputs.

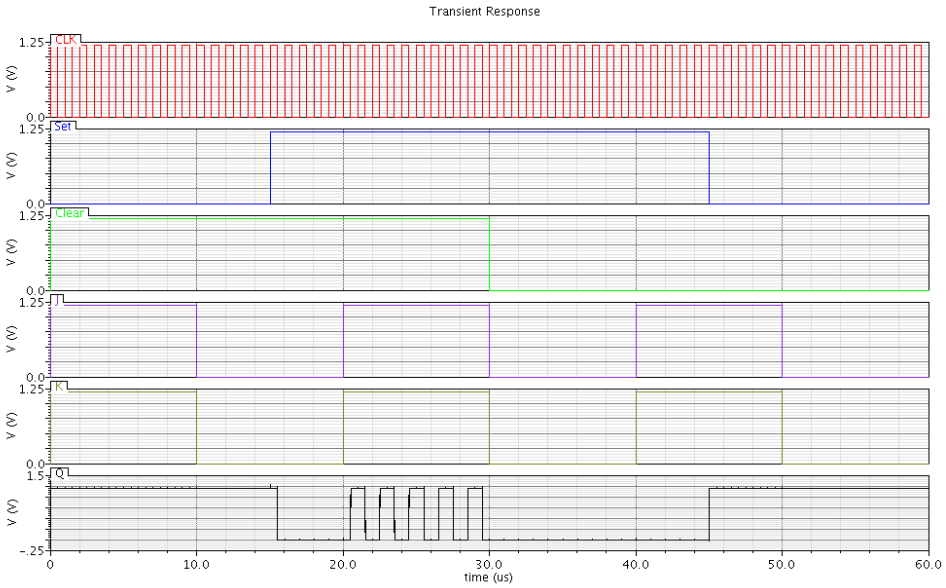

Figure 5.3 – Timing diagram of master-slave negative *JK* flip-flop with *set* and *clear*.

5.2. The Digital Counter

5.2.1. Synchronous 6-bit Up/Down Binary Counter

From Fig. 5.4, it can be analysed the transient response of the counter covered in this subchapter, according to *Set* and *Clear* inputs. When *Set* and *Clear* are booth enabled, the counter counts up, and it stops counting when *Set* and *Clear* are booth disabled, in this moment the counter "freezes" all *Q* outputs with value 1. If *Clear* remains inactive but *Set* is active, the counter "freezes" all *Q* outputs with value 0. The counting returns to normal operation when both *Set* and *Clear* become enabled. And when *Set* is off and *Clear* is on, the counter "freezes" again all *Q* outputs, with logic value 1.

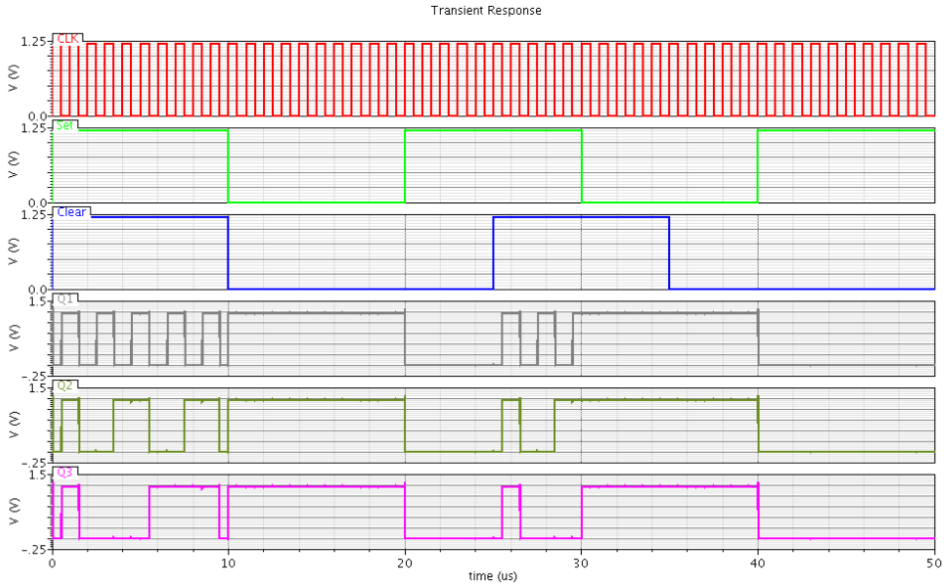

Figure 5.4 – Timing diagram of synchronous 6-bit up/down binary counter regarding *Set* and *Clear* inputs.

The behaviour of this counter concerning the *Up/Down* input is established in Fig. 5.5. When this input is enabled, the counter counts up, and at 50 us starts counting down, when *Up/Down* is disabled.

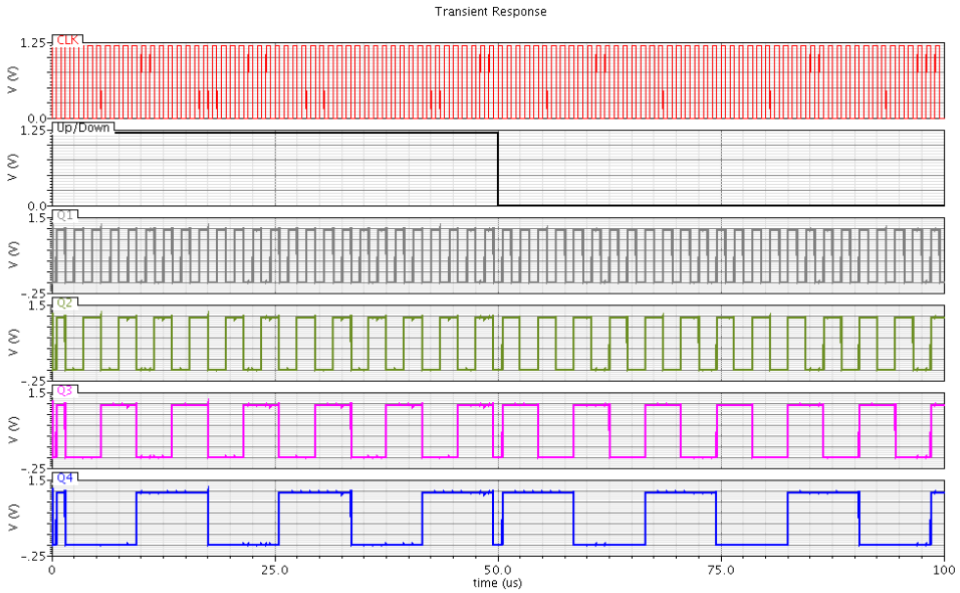

Figure 5.5 – Timing diagram of synchronous 6-bit up/down binary counter regarding *Up/Down* input.

5.3. Oscillators

5.3.1. Oscillator 1 (CCO 1)

For a capacitance of 1 pF in all three capacitors (C_1, C_2 and C_3), the current was varied from 500 nA to 300 uA obtaining frequencies from 0.57 MHz to 99.7 MHz. The graphic in Fig. 5.6, shows the evolution of frequency versus the input current variation.

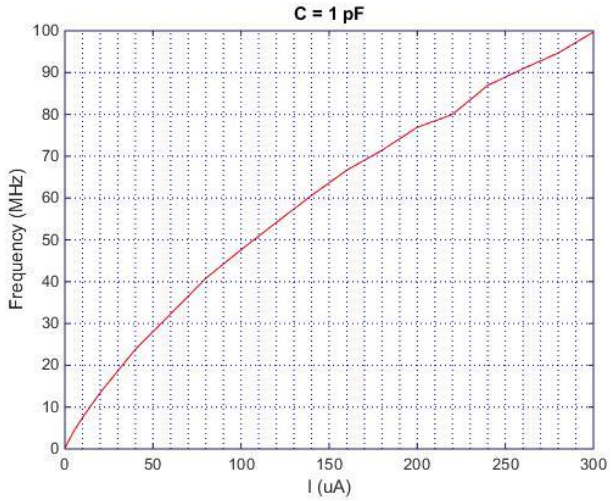

Figure 5.6 – Evolution of frequency versus the input current variation (C = 1 pF) for oscillator 1.

For a capacitance of 500 fF in all three capacitors (C_1, C_2 and C_3), the current was also varied spanning from 500 nA to 300 uA obtaining frequencies from 1.13 MHz to 195.92 MHz. The graphic in Fig. 5.7, shows the variation of the frequency with the input current sweep.

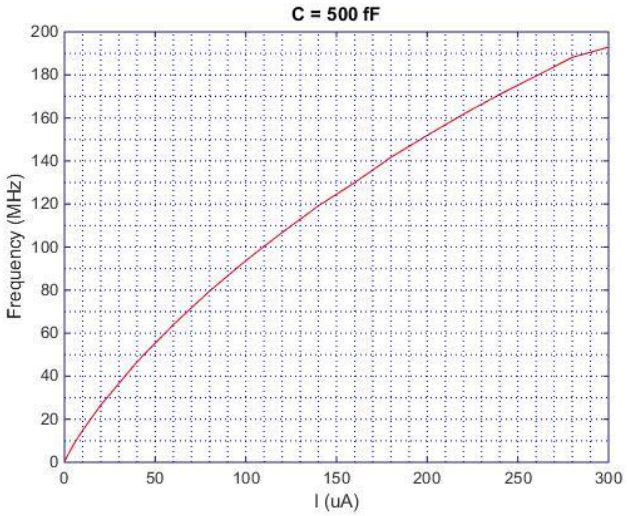

Figure 5.7 – Variation of frequency versus input current (C = 500 fF) for oscillator 1.

And finally, for a capacitance as small as 100 fF in all three capacitors (C_1, C_2 and C_3), the current was also varied ranging from 500 nA to 300 uA obtaining frequencies from 5.25 MHz to 894.40 MHz. The graphic in Fig. 5.8, shows the variation of frequency with the input current sweep.

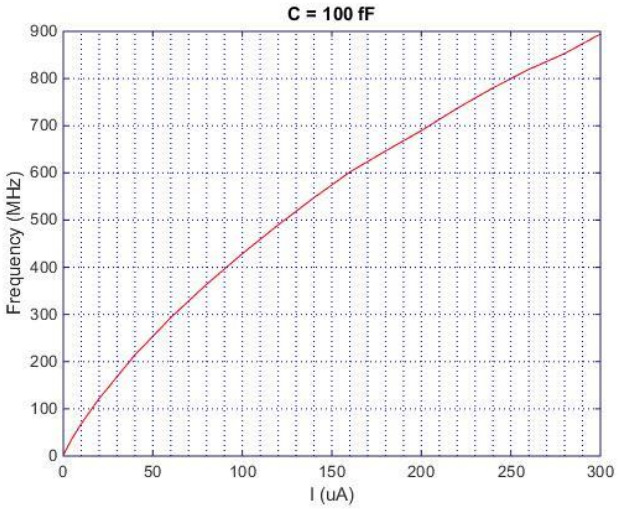

Figure 5.8 – Variation of frequency with the input current (C = 100 fF) for oscillator 1.

From those simulations, is perceptible that the variation of frequency with current variation is somehow linear, showing some evidence of the beginning of saturation (i.e., non linear behaviour) for currents from 250 uA upward.

Table 5.1**:** Amplitude response with current variation in oscillator 1.

Current (μA)	Amplitude (mV)
300	1025
280	1000
260	973
240	949
220	923
200	895
180	865
160	832
140	805
120	772
100	737
80	699
60	656
40	605
20	537
10	484
5	441
1	355
0.5	322

Moreover, it should be noted that, in all the three cases shown, the amplitude voltage of the oscillator's output with the different current variations reduce from 1.025 V to 322 mV, respectively to current reductions from 300 uA to 500 nA, as can be seen in Tab.5.1.

In Fig. 5.9 is shown a nominal simulation of this oscillator with I = 200 uA and all capacitance values set to 300 fF. The simulated frequency is 248.51 MHz with 893 mV of output amplitude. As mentioned above, in this configuration of oscillator the voltage amplitude vary with current and capacitors, although the variation with the current is much more effective.

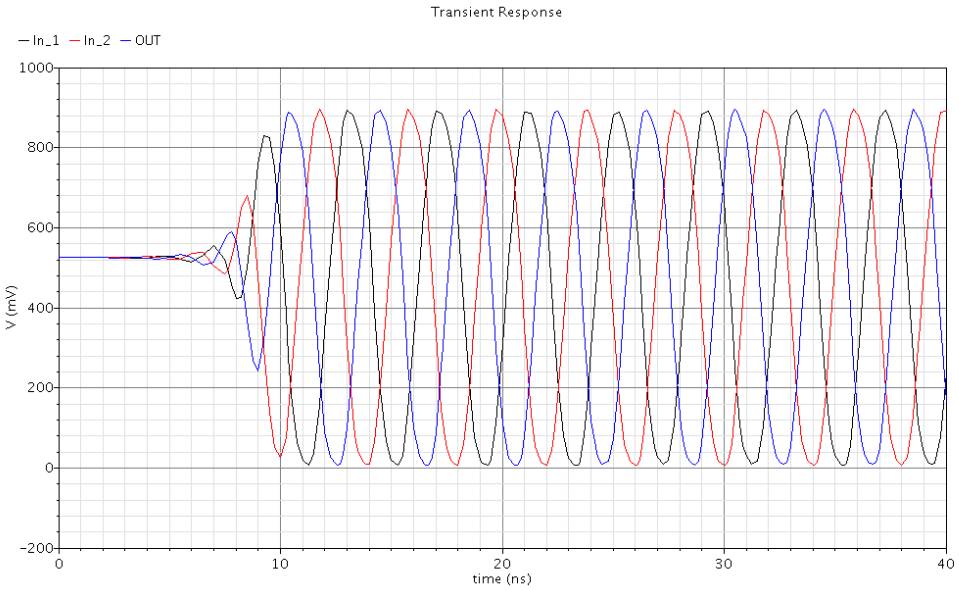

Figure 5.9 – Transient oscillation in the simulation run of oscillator 1.

5.3.2. Oscillator 2 (CCO 2)

The difference of this oscillator to the oscillator discussed in subchapter 5.3.1, is that in this oscillator the amplitude voltage always remains constant through current and capacitor variations, which can be explained by the presence of voltage source V_{in} between V_{DD} and gnd of the oscillator. In this circuit, the frequency only varies with current variation, as can be seen through observation of Fig. 5.10, Fig. 5.11 and Fig. 5.12. Also the upper and lower transistors in each inverter act as current source, limiting the current through each inverter.

For a capacitance of 1 pF in all three capacitors (C_1, C_2 and C_3), the current was varied from 500 nA to 300 uA obtaining frequencies from 0.11 MHz to 44.01 MHz. The graphic in Fig. 5.10, shows the variation of frequency with the input current variation.

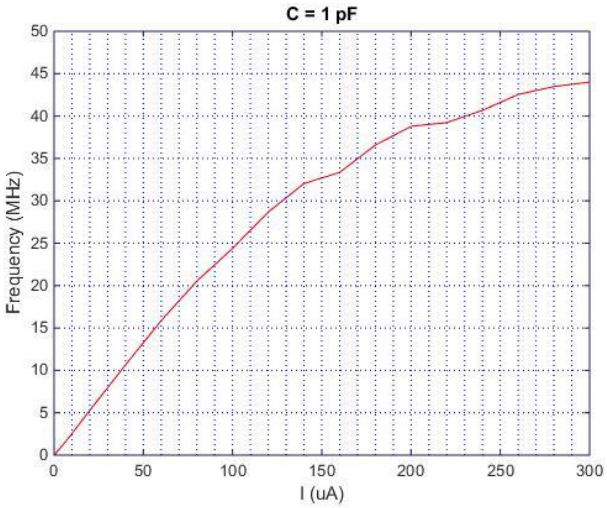

Figure 5.10 – Variation of frequency with current (C = 1 pF) for oscillator 2.

For a capacitance of 500 fF in all three capacitors (C_1, C_2 and C_3), the current was also varied spanning from 500 nA to 300 uA obtaining frequencies from 0.22 MHz to 88.51 MHz. The graphic in Fig. 5.11 shows the variation of the frequency versus the input current.

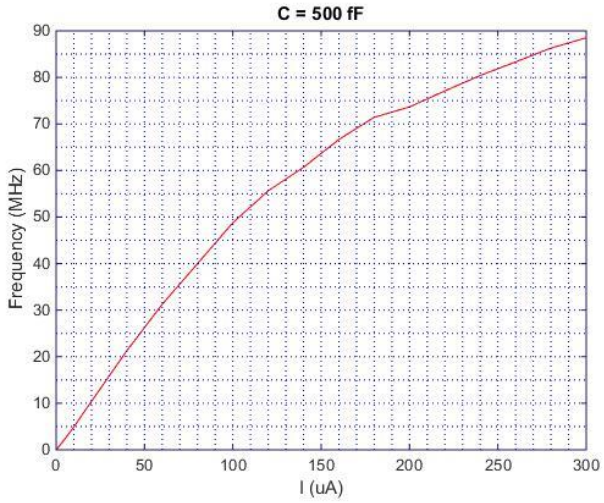

Figure 5.11 – Variation of frequency with the input current (C = 500 fF) for oscillator 2.

And finally, for a capacitance of 100 fF in all three capacitors (C_1, C_2 and C_3), the current was also varied ranging from 500 nA to 300 uA obtaining frequencies from 0.99 MHz to 410.17 MHz. The graphic in Fig. 5.12 shows the variation of the frequency with the input current.

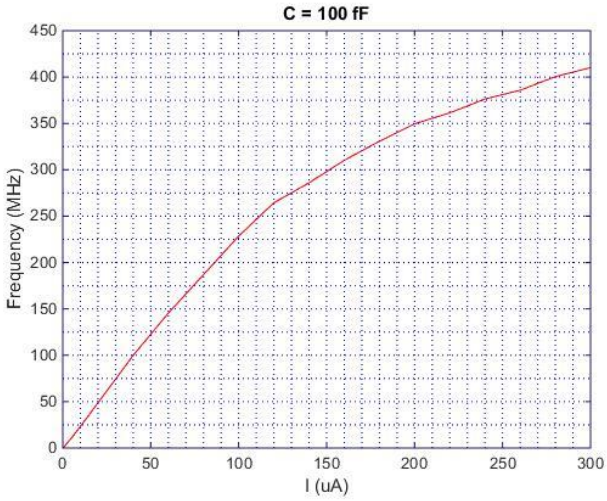

Figure 5.12 – Variation of frequency with current (C = 100 fF) for oscillator 2.

The variation of the frequency with the current sweep is similar concerning the design of curve, for the three cases, although there are significant differences in the values of the frequencies for each capacitance value.

The frequency curve for C = 100 fF seems to be the most linear, while for C = 1 pF appears to be more inconsistent, having two slight relapses, one at 150 uA ad other at 210 uA.

In Fig. 5.13 is presented a simulation of oscillator 2 with I = 200 uA and all capacitances of 300 fF, the same values of previous oscillator. The obtained nominal frequency was 122.31 MHz, a lower value concerning the oscillator 1, and as in this case we have an input voltage source imposing 1.2 V between *Vdd* and *ground*, the amplitude voltage in theory should also be 1.2 V, although this does not occur at all. The voltage amplitude in this case stays close to the voltage imposed by V_{in} with 1.15 V, but if we increase the current to 1 mA and decrease the capacitance to 100 fF, the output amplitude voltage will be the same 1.15 V with 535.91 MHz of frequency.

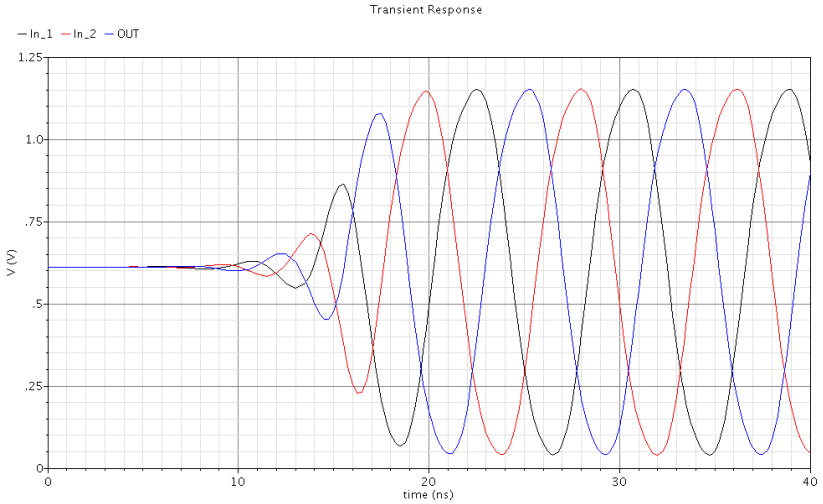

Figure 5.13 – Transient oscillation in the simulation run of oscillator 2.

5.3.3. Conclusion of oscillators

After the end of the simulations of both oscillators, it was decided to use oscillator 1, because the same can meet all the required specifications, is simpler in terms of construction, and it provides more appropriate curves of frequency response over the variation of the current for different values of capacitance. Besides the referred simplicity is also dissipates less power.

5.4. Transconductance Stage (*gm*)

The simulation results of the transconductance stage are mainly related with the DC operating point, accordingly to Tab.5.1. The drain current I_{ds} is split correctly through the transistors. As in all transistors $V_{GS} > V_{th}$ and $V_{DS} \geq V_{GS} - V_{th}$, the same are working in saturation (i.e., active region) mode. And all transistors have drain saturation voltage $(V_{dsat}) > 50\,mV$, proving that the same are working in strong inversion, assuring the proper operation of MOSFET in saturation mode after fabrication, and avoiding the sub-threshold regime (speed degradation although better power efficiency).

Table 5.2: DC operating point of all transistors of the transconductance stage.

Transistor	$I_{ds}(\mu A)$	$V_{gs}(mv)$	$V_{ds}(mv)$	$V_{th}(mv)$	$V_{dsat}(mv)$	$gm(\mu S)$
M_1	15.0002	271.112	271.112	265.961	69.012	330.656
M_2	15.0438	271.112	279.519	265.961	69.012	331.563
M_3	7.52183	320.481	361.849	319.278	68.9345	166.139
M_4	7.52183	320.481	361.849	319.278	68.9345	166.139
M_5	7.52202	358.633	255.514	358.235	71.3468	166.026
M_6	7.52202	358.633	255.514	358.235	71.3468	166.026
M_7	7.5218	303.119	303.119	270.89	76.4368	151.292
M_8	7.5218	303.119	303.119	270.89	76.4368	151.292

5.5. Digital-to-Analog Converter

5.5.1. The 6 bit IDAC

The simulated output voltage of the 6 bit IDAC looks like a negative stairway (starting at Vdd), comprising 64 steps. The expected 63 transitions, that represent the sum of all multiples of *W's* (32 + 16 + 8 + 4 + 2 + 1 = 63), as can be observed in Fig.5.14, showing that the same is working

as expected, having only a slightly larger gap at t = 16 us, that doesn't affect the desired monotonic characteristic and functionality of this building block.

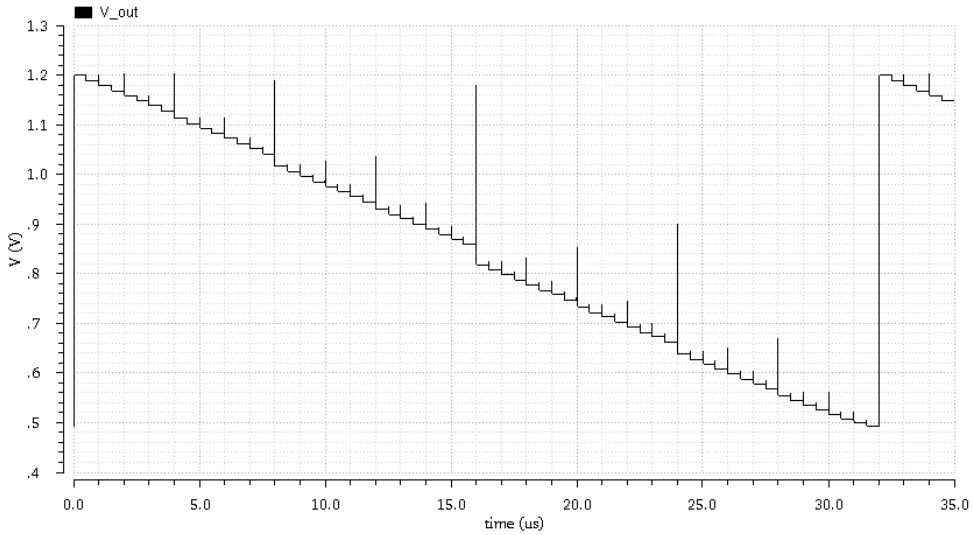

Figure 5.14 – Simulated output voltage of the 6 bit IDAC.

5.6. Electro-Thermal Filter (ETF)

In Fig. 5.15, the behaviour of the EFT with different values of $R_{1,2,3,4}$ can be observed. As it was previously referred in chapter 4, with $R_{1,2,3,4} = 0\ \Omega$ the expected phase shift should be 0º (Fig.5.15), and with $R_{1,2,3,4} = 30.5\ k\Omega$ the phase shift should be 45º (Fig.5.16), between input and output waves. The input of ETF was always driven with $V_{pulse} = 1.17\ MHz$ of frequency and 1.2 V of amplitude.

When the phase shift is 0º, both input and output waves are equal in shape (square waves) and amplitude, being superposed one on the other, as can be seen in Fig.5.15.

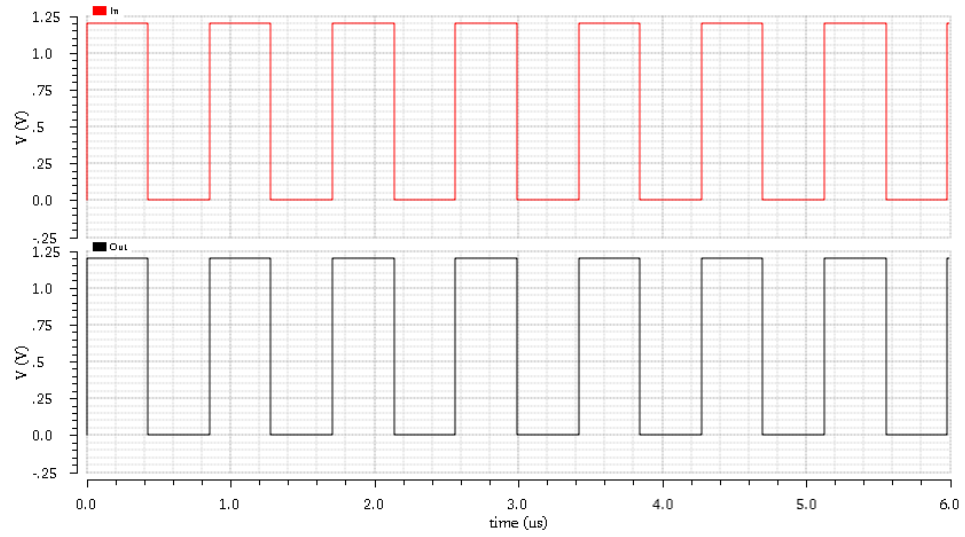

Figure 5.15 – Behaviour of ETF, between input and output waves, for phase shift of 0º.

When the phase shift is changed to 45º, beyond the referred phase shift, both input and output waves show differences in shape and amplitude. The output wave is sinusoidal and with less amplitude regarding to the input wave, as can be observed in Fig. 5.16. It should be noted that it was necessary to add a DC voltage source with 400 mV between all the capacitors along with output resistance, of the ETF, and the ground, in order to have enough amplitude height at the output of this EFT, to efficiently and properly drive the input differential pair of the transconductance stage.

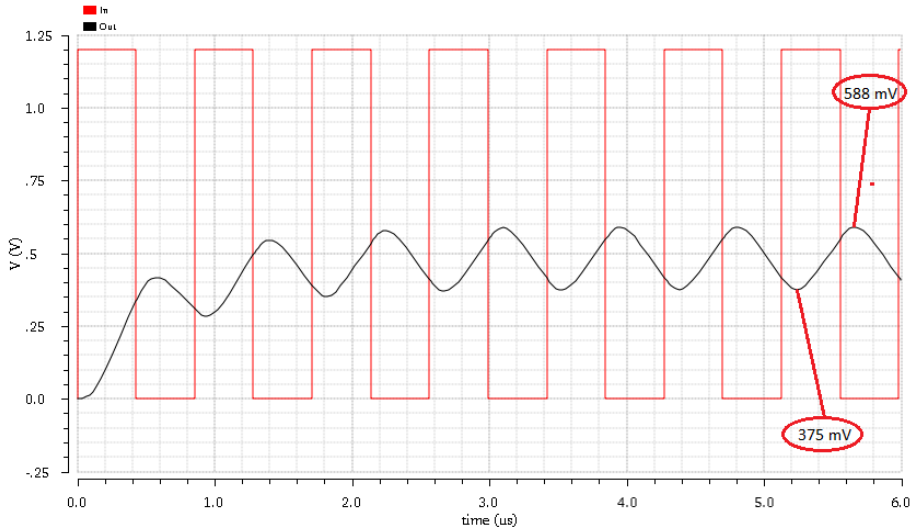

Figure 5.16 – Behaviour of ETF, between input and output waves, for phase shift of 45º.

From this simulation results can be concluded that this Electro-Thermal Filter (electrical model) behaves similarly as a low-pass RC filter, with the majority of resistances displayed in series, and capacitors in parallel, permitting to low-pass frequencies easily and reducing the amplitude of frequencies higher than the cut-off frequencies. The output amplitude was reduced from an input square wave of 1.2 V for a nearly 213 mV in a sinusoidal form, demonstrating the RC low-pass filtering behaviour of this ETF circuit model.

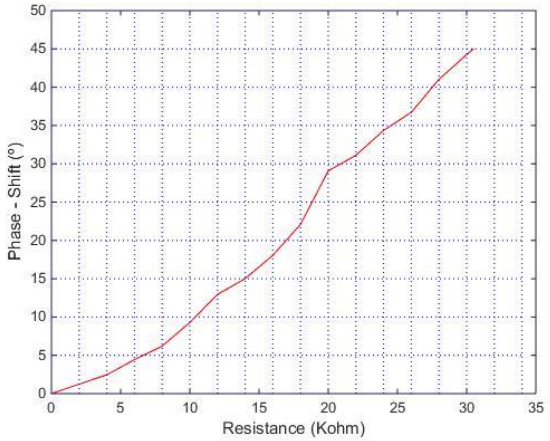

Figure 5.17 – Response of the ETF in terms of phase-shift, with resistance variation.

5.7. TDT Sensor – Open Loop

During the construction of the TDT Sensor it was necessary to test and simulate their blocks separately, and also connect them little by little in order to see if each of them work in harmony with other blocks loading each other.

Moreover, the progressive interconnecting of the different blocks is also presented throughout this subchapter.

5.7.1. Interconnecting the Transconductance stage and and the Oscillator (CCO 1)

The starting point is constituted by the transconductance stage and by the oscillator (CCO 1), where the first one is controlled by the two V_{pulse} sources, during a simulation time of 3 us, in order to see the behaviour of these two blocks, as it is illustrated in Fig.5.18. The total amplitude of V_{pulse} signals, that is 213 mV, which lies between 375 mV and 588 mV, serves to simulate the amplitude of the output wave of the Electro-Thermal Filter, in order to verify the behaviour of the differential pair of the transconductance stage coupled to the oscillator.

The current that feeds the differential pair was established in 15 uA, being a value that ensures a good response of oscillator, allowing a correct variation of the current-to-frequency gain of the same. Because there were made other simulation trials with higher values of the current that feeds the differential pair, but the oscillator's response was too sensitive, causing an abrupt reduction of frequency and amplitude, which would interfere in the operation of the 6 bit counter.

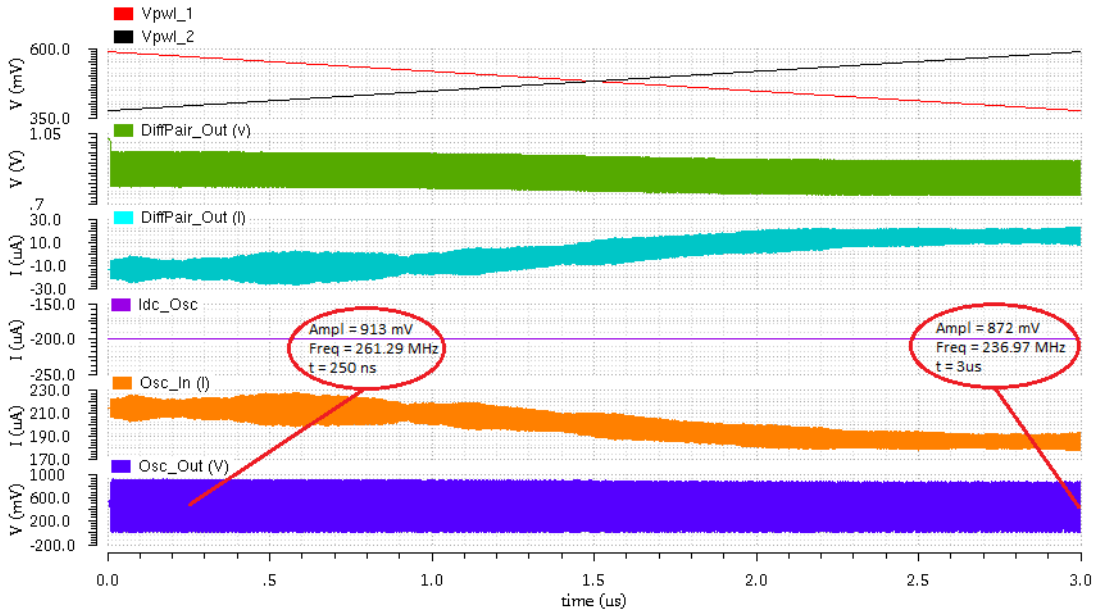

Figure 5.18 – Behaviour of differential pair and oscillator.

The output voltage of the transconductance stage seems to be stable, and the output of the oscillator shows some natural variation (in this case decrease) of the frequency from 261.29 MHz at T = 250 ns to 236.97 MHz at t = 3 us, and amplitude decrease from 913 mV at t = 250 ns to 872 mV at t = 3 us, as the input current of the oscillator is also decrease along these 3 us, showing that this oscillator has current-to-frequency gain as required in the specifications of this project.

5.7.2. Interconnecting the transconductance stage, the Oscillator (CCO 1) and the 6 bit Counter

As the clock is activated from the output wave of the oscillator, can be concluded that the amplitude or the "strength" of the signal at the output of the oscillator, that is around 800 mV, is enough to drive the next block, as it is shown in Fig.5.19.

After some attempts, this value of amplitude at the output of the oscillator was the minimum accepted to activate the clock in order to accomplish the bit count, corresponding to a current of 200 uA at the input of the oscillator (CCO 1).

It should be noted that, after connecting the 6 bit counter to the oscillator (CCO 1), the amplitude and the frequency output of this last block has decreased slightly, now being 231.73 MHz at t = 250 ns and 210.53 MHz at t = 3 us in terms of frequency, and being 854 mV at t = 250 ns and 813 mV at t = 3 us in terms of amplitude. This small decrease of the frequency and amplitude at the output of the oscillator with the presence of the counter occurs because of the expected loading effect.

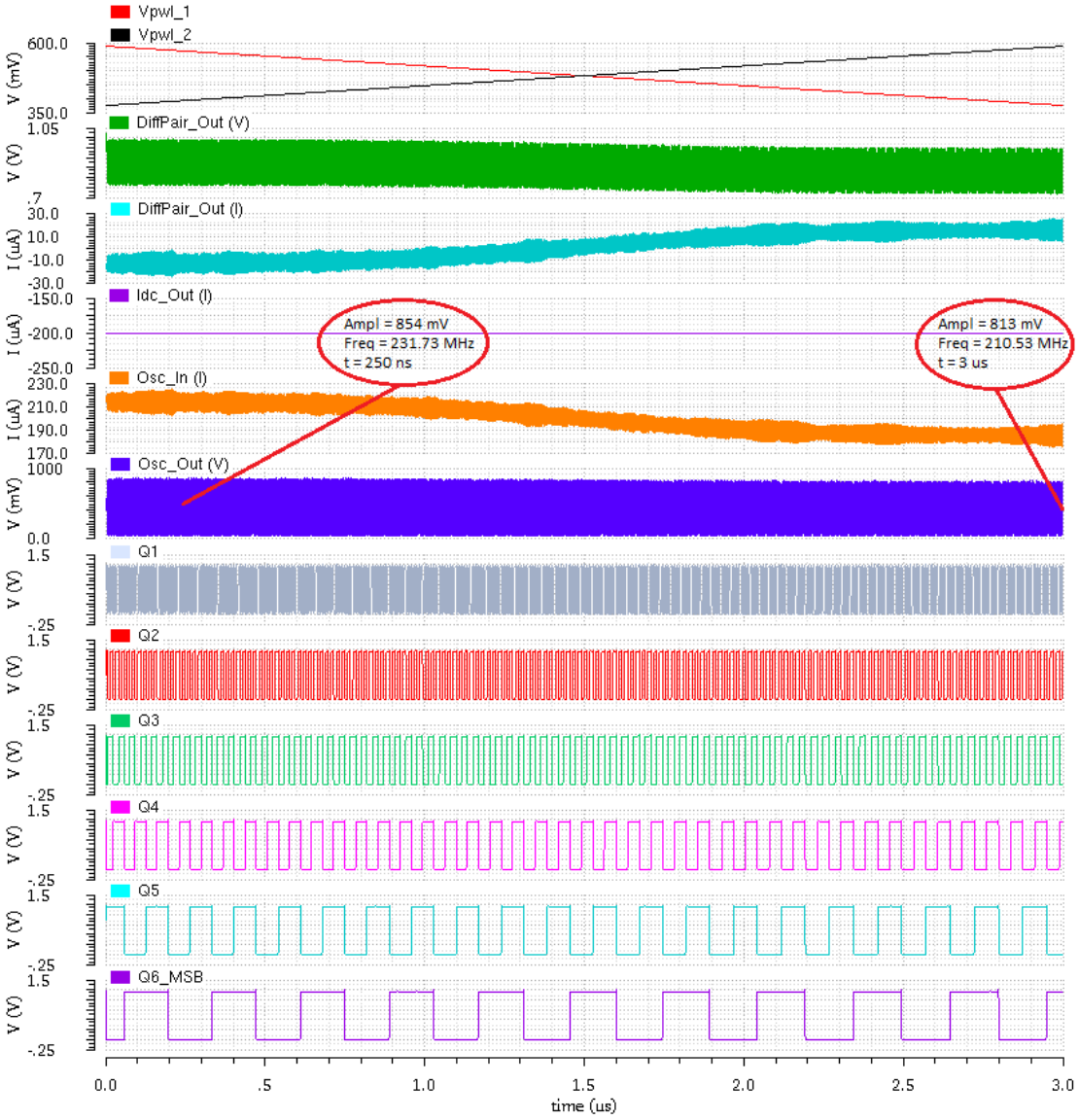

Figure 5.19 – Simulated behaviour of the transconductance stage, oscillator and 6 bit counter.

5.7.3. Interconnecting the ETF, the transconductance stage, the Oscillator (CCO 1), the 6 bit Counter and the two backend *D* Flip-Flops

When the Electro-Thermal Filter is included, it substituted the two V_{pulse} sources, presented in the two last subchapters, serving as inputs for the transconductance stage. As can be seen in Fig.5.20, the input of the transconductance stage is now coming from the output of the ETF, that is a sinusoidal wave but with the same amplitude of the two V_{pulse} sources, being about 213 mV. Should be noted that the phase shift of the ETF is 45º.

The behaviour of the differential pair is similar in this case, with the range of amplitude identical compared to the presented in Fig.5.18 and Fig.5.19. Should be noted that the shape of

the output wave of the ETF is reflected on the shape of the output amplitude of the transconductance stage, that in this case resembling a “wave effect”.

This “wave effect” is also reflected at the output current of the differential pair and at the input current of the oscillator, which will be slightly reflected in some variation of amplitude and frequency at the output of this last one block.

The amplitude and the frequency at the output of the oscillator vary from 209.93 MHz to 222.81 MHz in terms of frequency, and between 810 mV and 835 mV in terms of amplitude.

Moreover, it is added a *D* flip-flop after the counter through MSB (most significant bit) wire. The driving clock of the *D* flip-flop was set to 37.5 MHz, half the frequency that was used to simulate and analyse the FFT of the total schematic of the circuit presented in the next section of this chapter.

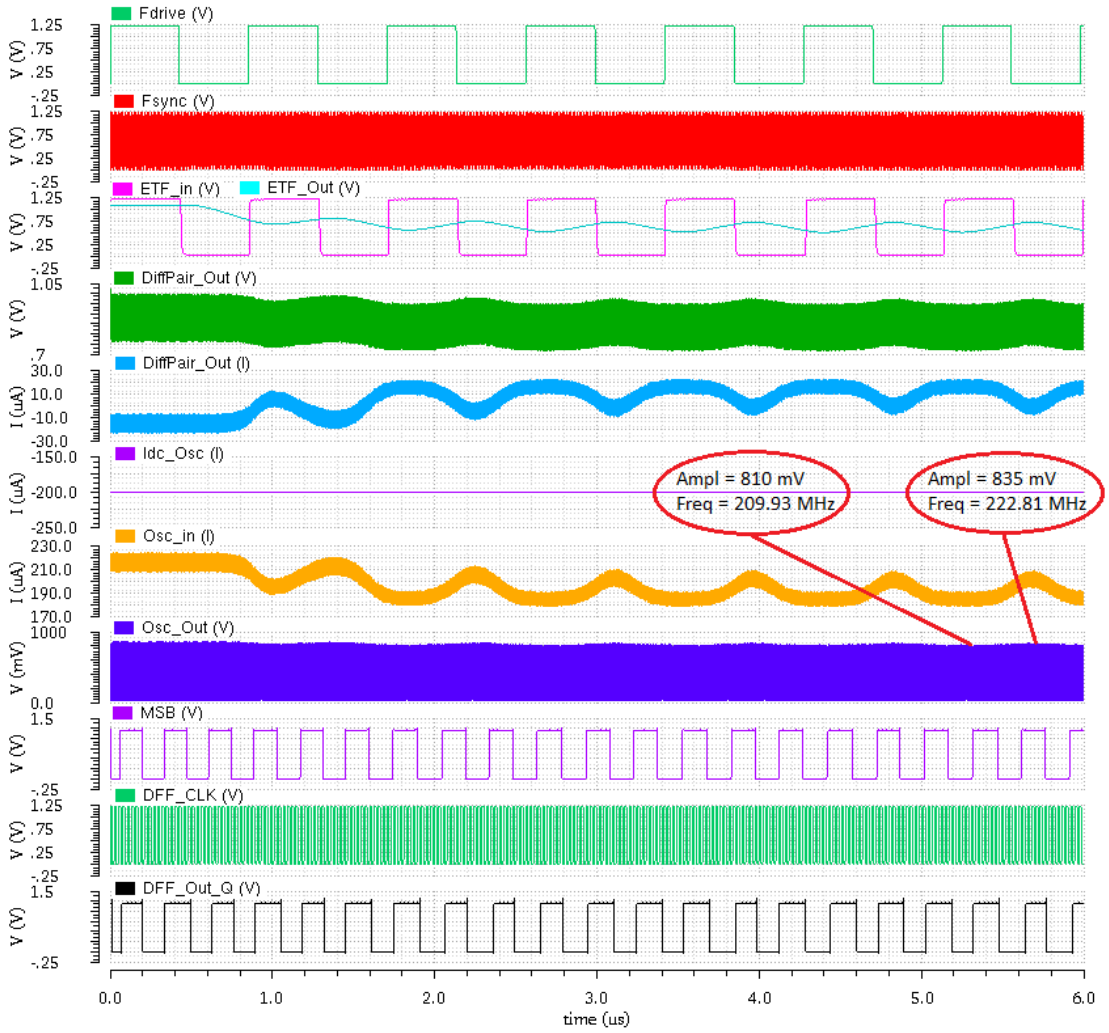

Figure 5.20 – Simulated behaviour of ETF (phase shift = 45º), transconductance stage, oscillator, 6 bit counter and two *D* flip-flops.

5.8. TDT Sensor – Closed Loop Simulations

This is the final step in building the TDT Sensor system. To close the loop, two *D* flip-flops have been added to complete the final circuit schematic. The first *D* flip-flop is coupled with two switches controlled by one V_{pulse} source each one, and is connected between the output of the TDT Sensor in open loop configuration and the *Up/Down* input of the 6 bit counter. An additional *D* flip-flop has also been added at the input of the ETF.

In Fig.5.21 it is shown the final and complete circuit schematic of the thermal-diffusivity temperature sensor system in closed loop configuration. This circuit is represented as it was implemented in Cadence Virtuoso for simulations, with all the details at the level of voltage and current sources, with the respective values of their magnitudes. It comprises the ETF, the Gm stage, the CCO, the 6-bit Counter, 3 *D*-type Flip-flops and several switches. IDAC block has been designed and it connects directly to the output of the transconductance stage. However, since it is only used for calibration purposes, it has not been included here.

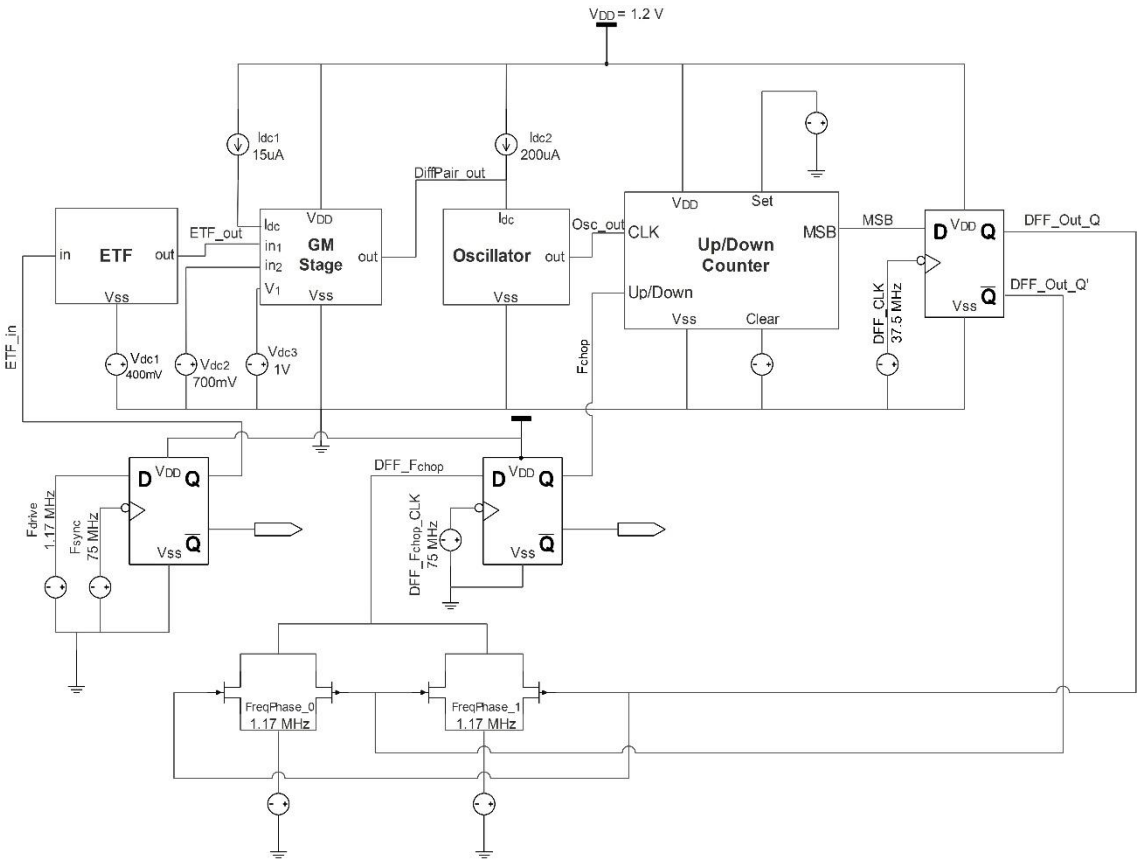

Fig. 5.21 – Circuit schematic of the complete TDT Sensor System.

Regarding the first *D* flip-flop, with switch, the first V_{pulse} source connected to the first switch has a reference 1.17 MHz clock (Fϕ0) with phase shift ϕ0 = 0º, and the second V_{pulse} source connected to the second switch has also a reference 1.17 MHz clock (Fϕ1) with phase shift ϕ1 = 90º, spanning the phase range from 0º to 90º in order to cover the full temperature range .

The second *D* flip-flop is also controlled by an external 75 MHz clock (Fsync) to generate a 1.17 MHz ETF driving signal (*Fdrive*). This *Fdrive* signal enters at the input of this *D* flip-flop and after a minimum phase shift resulting from the presence of *Fsync*, leaves the same flip-flop with an equal frequency, to then enter the ETF.

5.8.1. Complete Schematic of TDT Sensor

In this final step of simulation of the TDT Sensor circuit in closed-loop configuration, can be seen the most important components operating together, where the square wave at the input of the ETF (ETF_in (V)) comes out with a phase shift of 45º (ETF_Out (V)) and attenuated in terms of amplitude because of "RC Filter effect" produced by this ETF configuration. Then we have the transconductance stage that amplifies the output of the ETF (DiffPair_Out (V)) and also produces a certain current value (DiffPair_Out (I)) which is then added along with the current from the oscillator's source (Osc_in (I)), to this 3 ring oscillator in order to produce a certain amplitude and frequency at the output (Osc_Out (V)), that is dependent of this sum of currents. The oscillator's output enters to 6 bit counter where the same through MSB output "attacks" the first *D* flip-flop. The *Set* and *Clear* inputs of the counter are always *on*. The output signals (DFF_Out_Q (V)) and its complement (DFF_Out_Q' (V)) of this first *D* flip-flop are slightly phase shifted due to the presence of the sampling rate (DFF_CLK (V)) that is 37.5 MHz. Then, those signals enter to interruptor 1 (Fϕ0) and interruptor 2 (Fϕ1). Those interruptors are phase shifted by 90º to cover the full temperature range, and at their output the signal (DFF_Fchop (V)) along with signal (DFF_Fchop_CLK (V)) enter to the second *D* flip-flop whose output (F_chop (V)) enters to the 6 bit counter through *Up/Down* input of the same, as can be observed in Fig.5.22.

In Fig.5.23 it is presented the FFT of the output bitstream during a fine conversion. As the noise shaping has a slope of 20 dB/dec, around a frequency of 10^7 MHz, it is proved that the TDT Sensor circuit works properly in simulation and in closed-loop. It is not possible to see an continuous inclination of the noise shaping until the end of the graphic, because it is not applied a real signal to the TDT Sensor, and also, are presented 15000 samples of the FFT graph, which are enough to see if the circuit works, but are insufficient to a more specialized analysis of the same.

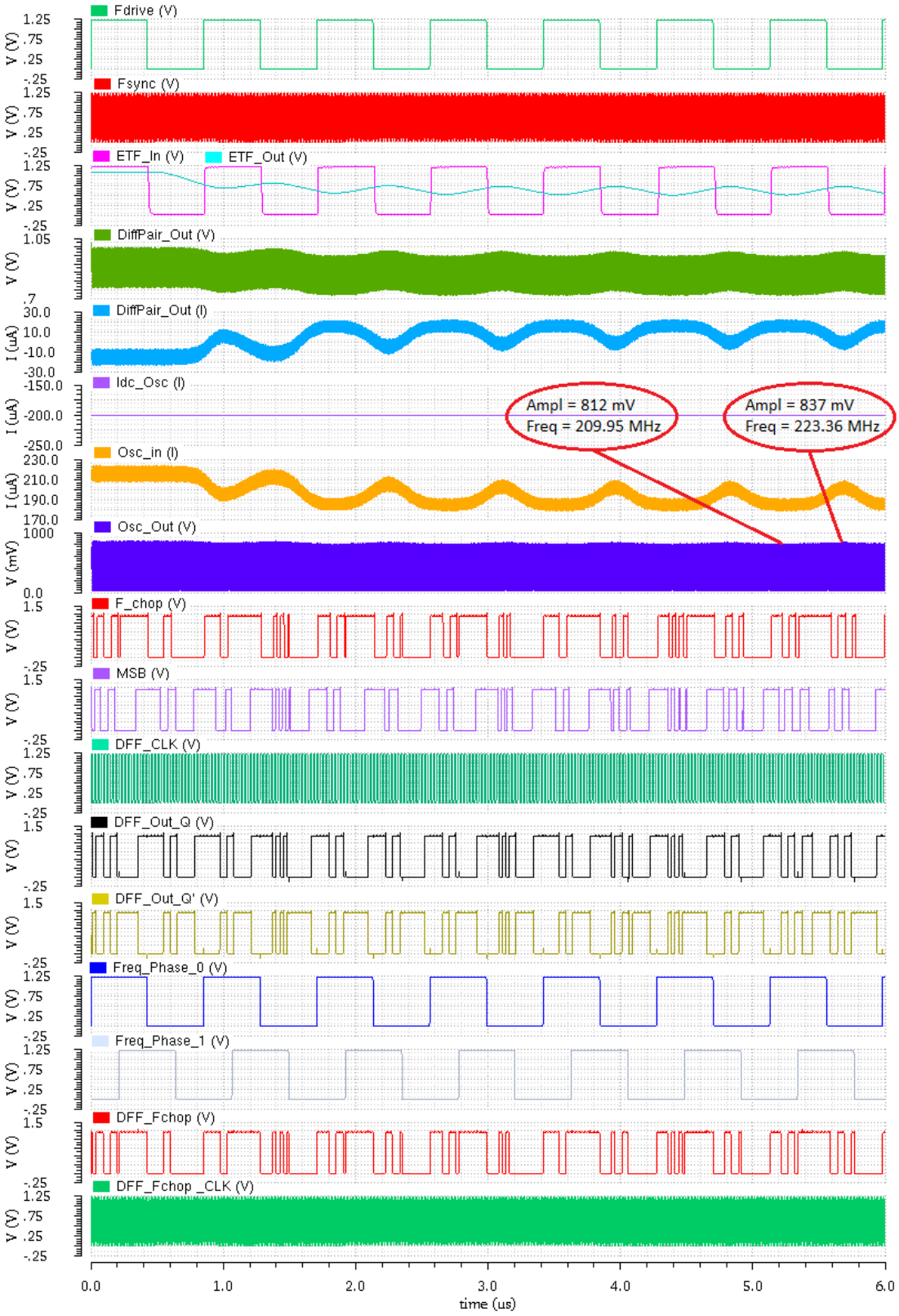

Figure 5.22 – Simulated behaviour of the complete circuit of TDT Sensor in closed-loop configuration.

Along the FFT output bit-stream there are two instantaneous peaks in the second half of the range frequency between 10^6 MHz and 10^7 MHz, that can be explained by the frequency of the sampling rate (Fs) that was established in 75 MHz, in order to analyse the FFT points of the simulation results, and the MATLAB algorithm that was used to automatically process all the FFT points of the simulation results. This MATLAB algorithm generates an close approximation of the real FFT, and the use of the same algorithm was necessary due to many samples that was necessary to analyse, and making this task almost impossible to be performed manually.

In the other hand, the sampling rate (Fs) was established in 75 MHz instead of 1.17 MHz in order to be possible to analyse a minimum set of FFT samples without resorting to very long simulations.

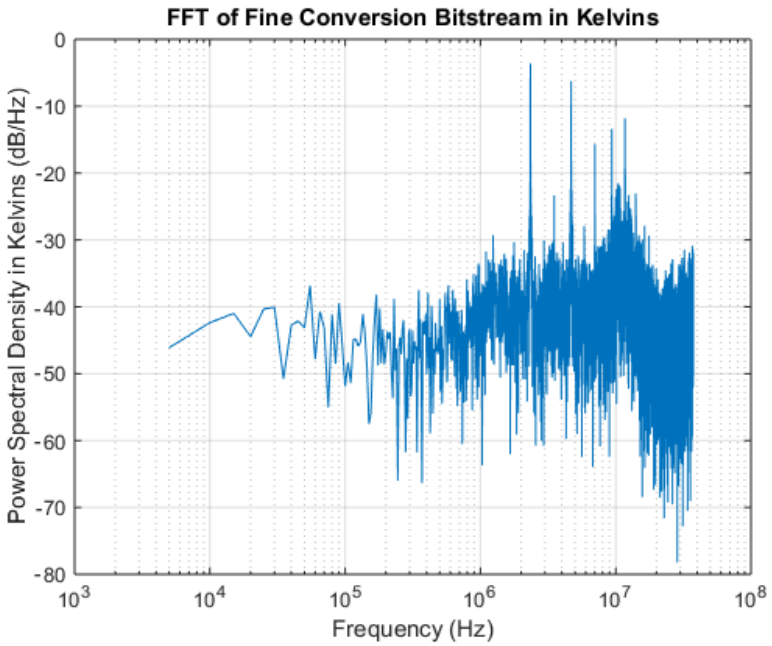

Figure 5.23 – Simulated FFT of the phase-domain ΔΣ modulator bit-stream during fine conversion with 15000 samples.

Chapter

Conclusions and Future Work

6

6.1. Conclusions

The main objective of this thesis was to study and demonstrate the constitution and operation of the thermal-diffusivity temperature sensor designed in a 0.13 μm standard CMOS technology, operating at 1.2 V. Also are presented the mathematical equations of various blocks, with theoretical explications and final simulation results of each one, and simulations of the entire TDT Sensor circuit in a closed-loop configuration.

Although it has been also designed and sized, the only circuit block that was not used in the final TDT Sensor circuit simulations was the 6 bit IDAC. It wasn't necessary connect it because this thesis work is based on theoretical simulations, without a really physical implementation of this sensor in a real life, making unnecessary either the trimming or calibration of this device.

Through FFT (Fast Fourier Transform) simulation results it was concluded that the final circuit of the sensor behaves as expected, presenting an noise shaping with the predicted first-order slope of 20 dB/dec.

The thesis work of this TDT Sensor circuit was based on a original thermal-diffusivity temperature sensor presentation described in [48], along with a comparative table (Tab.6.1) of results of this original sensor circuit with other sensors intended for microprocessor monitoring. Due to the additional delay and thermal noise introduced by the CCO, the accuracy and resolution of this original sensor are a little affected regarding to previous TD sensor using a more analog read-out [5]. But, it is still more precise than other state-of-the-art BJT or delay-based temperature sensors for thermal monitoring applications, after a one-point-trim. Moreover, this highly digital read-out architecture permits small dimensions for this sensor, despite its realization in a well known 0.16 μm CMOS technology.

Table 6.1: Performance summary and comparison with other sensors works.

	This Work	[1]	[1]	[2]	[3]	[4]	[5]
Technology	130nm	32nm	22nm	32nm	65nm	32nm	160nm
Sensor Type	TD	BJT	BJT	BJT	Delay	Diode	TD
Inaccuracy (3σ) Untrimmed	±6.5ºC (expected)	-	-	±5ºC	-	-	±2.4ºC
Single Temp. Trim	±1.5ºC (with the designed IDAC)	±4.5ºC	-	-	±1.5ºC	-	±0.65ºC
Two Temp. Trim	-	±1.2ºC	±1.5ºC	-	-	±1.95ºC	-
Temp. Range	-10 – 125ºC (targeted)	20 – 110ºC	-10 – 110ºC	-10 – 110ºC	0 – 110ºC	0 – 100ºC	-40 – 125ºC
Area (mm^2)	N/A (layout not done)	0.02	0.006	0.02	0.008	0.001	0.008
Resolution (RMS)	0.6ºC (expected)	0.19ºC	0.25ºC	0.15ºC	0.94ºC	0.25ºC	0.2ºC
Speed	0.9kS/s	2kS/s	1.4kS/s	1.2kS/s	469kS/s	2.5kS/s	1kS/s
Power	3.6mW	3.78mW	1.35mW	1.6mW	0.5mW	0.5mW	3.1mW

6.2. Future Work

As a future work, the main goal is try to reduce the sensor's size to the maximum possible, taking advantage of the constant CMOS scaling. Because, in this type of temperature sensor the digital circuitry occupies 70% of the sensor's area, and porting it for example from 160 nm technology to a 32 nm process, should reduce the digital area (roughly) by 20 times, reducing the total sensor's area by an expected factor of about 4.

Furthermore, power consumption can be further improved, along with untrimmed inaccuracy and the resolution (in RMS).

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